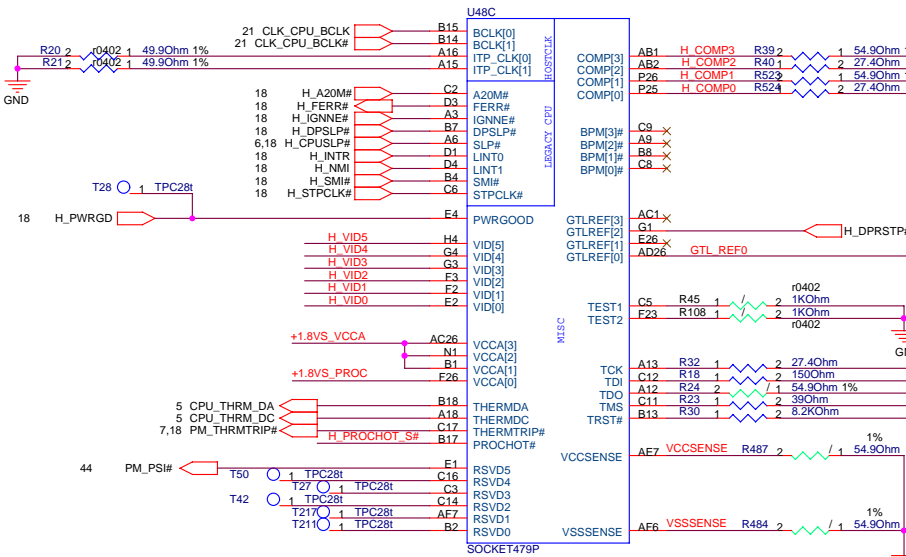
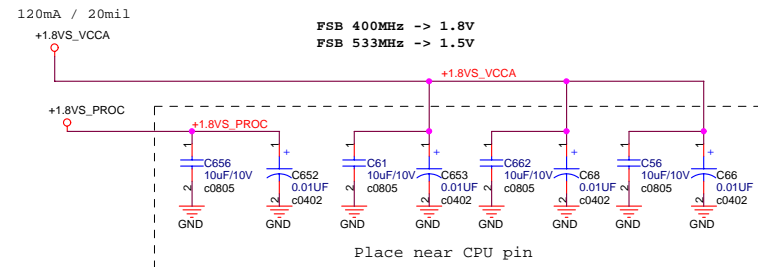


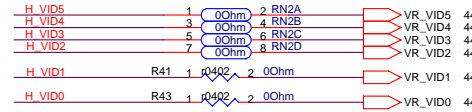
Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"



		A-STEP		B-STEP
Bclk	FSB	BSEL1	BSEL0	BSEL0
100	400	0	0	1
133	533	0	1	0

Dothan FSB533			
	Min	Typ	Max
VCCA	1.425V	1.5V	1.575V
ICCA			120mA



Dothan FSB533				
	LFM	TYP	HFH	
VCC	1.14V	1.2V	1.356V	
C4		C3	C0	
ICC	0.9A	7.59A	27A	

MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0 0	1.708V	1 0 0 0 0 0	1.196V
0 0 0 0 0 1	1.692V	1 0 0 0 0 1	1.180V
0 0 0 0 1 0	1.676V	1 0 0 0 1 0	1.164V
0 0 0 0 1 1	1.660V	1 0 0 0 1 1	1.148V
0 0 0 1 0 0	1.644V	1 0 0 1 0 0	1.132V
0 0 0 1 0 1	1.628V	1 0 0 1 0 1	1.116V
0 0 0 1 1 0	1.612V	1 0 0 1 1 0	1.100V
0 0 0 1 1 1	1.596V	1 0 0 1 1 1	1.084V
0 0 1 0 0 0	1.580V	1 0 1 0 0 0	1.068V
0 0 1 0 0 1	1.564V	1 0 1 0 0 1	1.052V
0 0 1 0 1 0	1.548V	1 0 1 0 1 0	1.036V
0 0 1 0 1 1	1.532V	1 0 1 0 1 1	1.020V
0 0 1 1 0 0	1.516V	1 0 1 1 0 0	1.004V
0 0 1 1 0 1	1.500V	1 0 1 1 0 1	0.988V
0 0 1 1 1 0	1.484V	1 0 1 1 1 0	0.972V
0 0 1 1 1 1	1.468V	1 0 1 1 1 1	0.956V
0 1 0 0 0 0	1.452V	1 1 0 0 0 0	0.940V
0 1 0 0 0 1	1.436V	1 1 0 0 0 1	0.924V
0 1 0 0 1 0	1.420V	1 1 0 0 1 0	0.908V
0 1 0 0 1 1	1.404V	1 1 0 0 1 1	0.892V
0 1 0 1 0 0	1.388V	1 1 0 1 0 0	0.876V
0 1 0 1 0 1	1.372V	1 1 0 1 0 1	0.860V
0 1 0 1 1 0	1.356V	1 1 0 1 1 0	0.844V
0 1 0 1 1 1	1.340V	1 1 0 1 1 1	0.828V
0 1 1 0 0 0	1.324V	1 1 1 0 0 0	0.812V
0 1 1 0 0 1	1.308V	1 1 1 0 0 1	0.796V
0 1 1 0 1 0	1.292V	1 1 1 0 1 0	0.780V
0 1 1 0 1 1	1.276V	1 1 1 0 1 1	0.764V
0 1 1 1 0 0	1.260V	1 1 1 1 0 0	0.748V
0 1 1 1 0 1	1.244V	1 1 1 1 0 1	0.732V
0 1 1 1 1 0	1.228V	1 1 1 1 1 0	0.716V
0 1 1 1 1 1	1.212V	1 1 1 1 1 1	0.700V

VCC

GND

Dothan FSB533			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
ICC		Max	2.5A

1.0V - 1.2V(+/- 5%)
S0-S1M: 2.5
A(CPU,MCH,ICH)

+VCCP (CPU) Decoupling Capacitor
(Place near CPU)

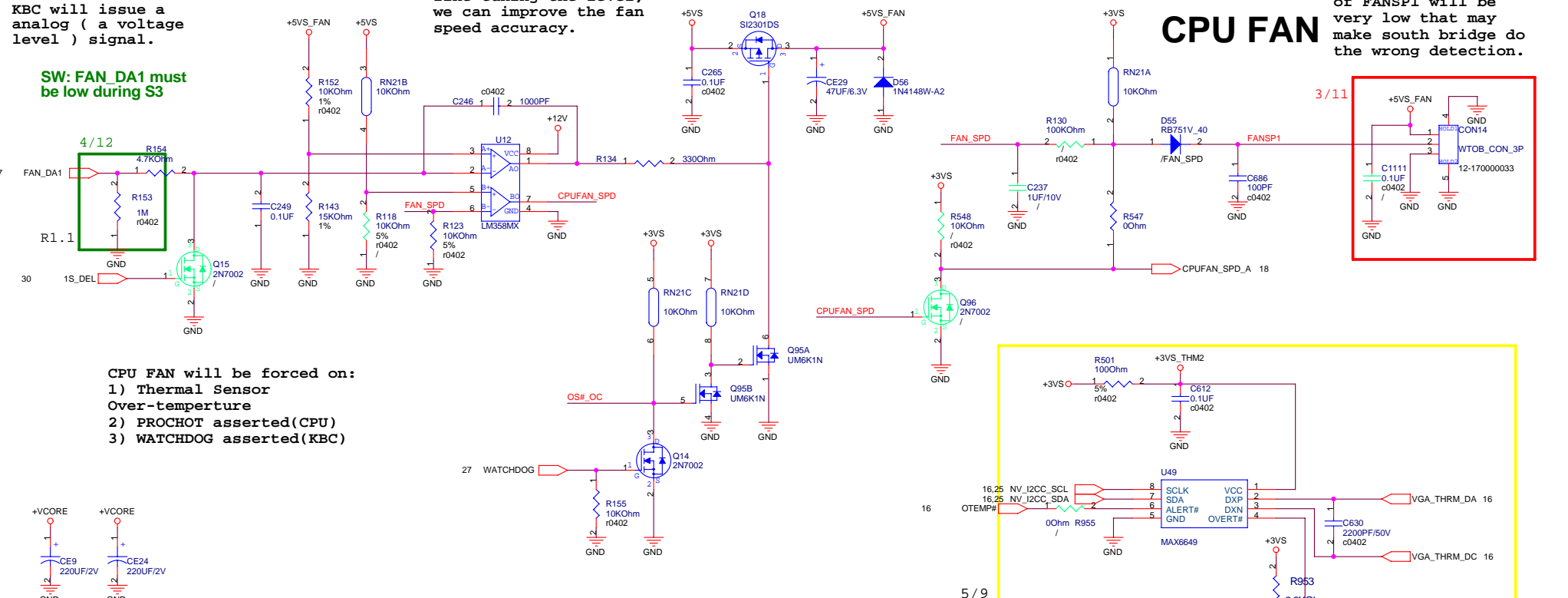
Fan Speed Control

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

KBC will issue a
analog (a voltage
level) signal.

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

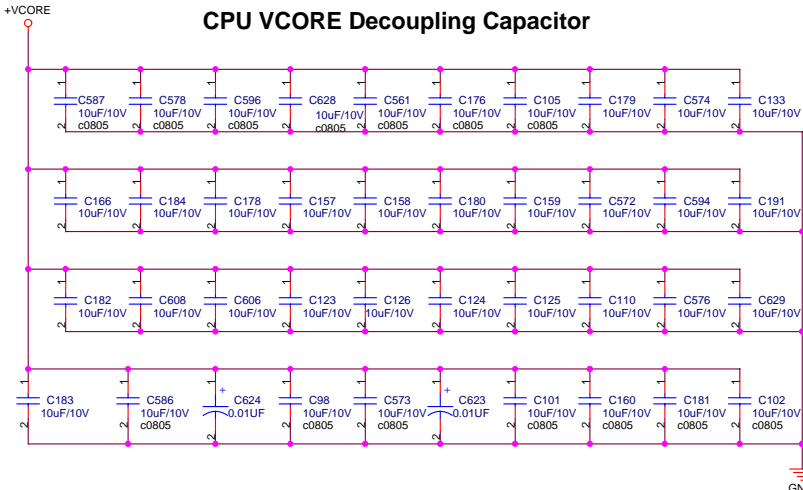
SW: FAN_DA1 must be low during S3



CPU FAN will be forced on:

- 1) Thermal Sensor Over-temperature
- 2) PROCHOT asserted(CPU)
- 3) WATCHDOG asserted(KBC)

CPU VCORE Decoupling Capacitor



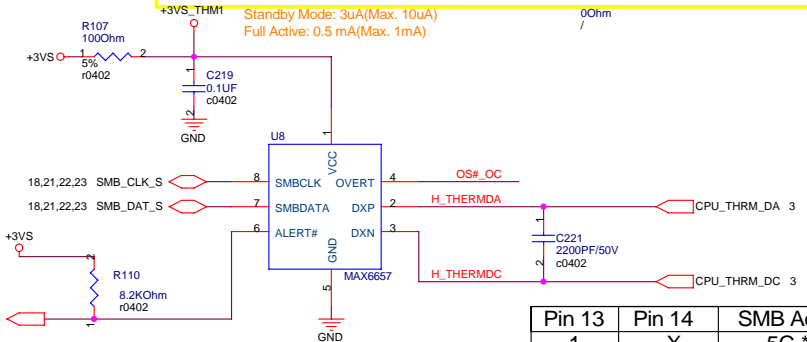
Mid Frequency
Decoupling (Place
around
Processor)

High Frequency
Decoupling (Place
underneath
Processor) using
10uF/6.3V X5R

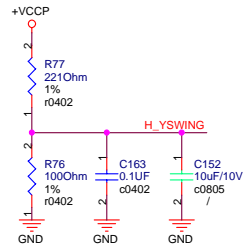
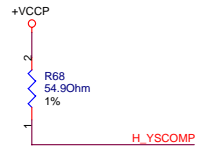
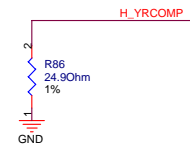
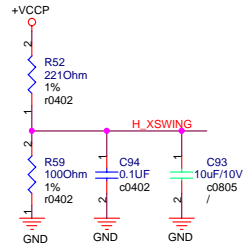
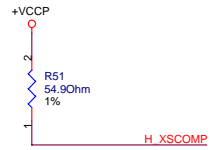
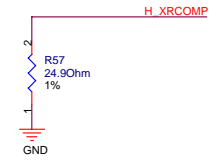
+V CORE
Bulk
Decoupling

Close to Pin A18
& B18 of CPU

**Four 200 uF are
located in
IMVP4**



Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58



3 H_D#[0..63]

H_D#0	E4	HD0#
H_D#1	E1	HD1#
H_D#2	F4	HD2#
H_D#3	HZ	HD3#
H_D#4	E2	HD4#
H_D#5	F1	HD5#
H_D#6	E3	HD6#
H_D#7	KZ	HD7#
H_D#8	D3	HD8#
H_D#9	F2	HD9#
H_D#10	J7	HD10#
H_D#11	J8	HD11#
H_D#12	H6	HD12#
H_D#13	F3	HD13#
H_D#14	K8	HD14#
H_D#15	H5	HD15#
H_D#16	H1	HD16#
H_D#17	H2	HD17#
H_D#18	K5	HD18#
H_D#19	K6	HD19#
H_D#20	J4	HD20#
H_D#21	G3	HD21#
H_D#22	H3	HD22#
H_D#23	J1	HD23#
H_D#24	L5	HD24#
H_D#25	K4	HD25#
H_D#26	J5	HD26#
H_D#27	E7	HD27#
H_D#28	L7	HD28#
H_D#29	J3	HD29#
H_D#30	P5	HD30#
H_D#31	L3	HD31#
H_D#32	L7	HD32#
H_D#33	V6	HD33#
H_D#34	R6	HD34#
H_D#35	R5	HD35#
H_D#36	P3	HD36#
H_D#37	T8	HD37#
H_D#38	R7	HD38#
H_D#39	R8	HD39#
H_D#40	U8	HD40#
H_D#41	R4	HD41#
H_D#42	T4	HD42#
H_D#43	T5	HD43#
H_D#44	R1	HD44#
H_D#45	T3	HD45#
H_D#46	V8	HD46#
H_D#47	U6	HD47#
H_D#48	W6	HD48#
H_D#49	U3	HD49#
H_D#50	V5	HD50#
H_D#51	W8	HD51#
H_D#52	W7	HD52#
H_D#53	U2	HD53#
H_D#54	U1	HD54#
H_D#55	Y5	HD55#
H_D#56	Y2	HD56#
H_D#57	V4	HD57#
H_D#58	Y7	HD58#
H_D#59	W1	HD59#
H_D#60	W3	HD60#
H_D#61	Y3	HD61#
H_D#62	Y6	HD62#
H_D#63	W2	HD63#

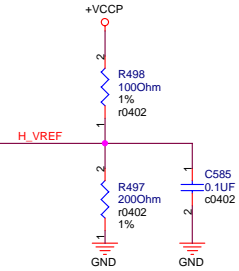
H_XRCOMP C1
H_XSCOMP C2
H_XSWING D1
H_YRCOMP T1
H_YSCOMP L1
H_YSWING P1

ALVISO_BGA1257

HOST

HA3#	G9	H_A#3
HA4#	C9	H_A#4
HA5#	E9	H_A#5
HA6#	B7	H_A#6
HA7#	A10	H_A#7
HA8#	F9	H_A#8
HA9#	D8	H_A#9
HA10#	B10	H_A#10
HA11#	E10	H_A#11
HA12#	G10	H_A#12
HA13#	D9	H_A#13
HA14#	E11	H_A#14
HA15#	F10	H_A#15
HA16#	G11	H_A#16
HA17#	G13	H_A#17
HA18#	C10	H_A#18
HA19#	C11	H_A#19
HA20#	D11	H_A#20
HA21#	C12	H_A#21
HA22#	B13	H_A#22
HA23#	A12	H_A#23
HA24#	F12	H_A#24
HA25#	G12	H_A#25
HA26#	E12	H_A#26
HA27#	C13	H_A#27
HA28#	B11	H_A#28
HA29#	D13	H_A#29
HA30#	A13	H_A#30
HA31#	F13	H_A#31
HADS#	F8	H_ADS#
HADSTB0#	D8	H_ADSTB#0
HADSTB1#	E13	H_ADSTB#1
HVREF	J11	H_VREF
HBNR#	A5	H_BNR#
HBPR#	D5	H_BPR#
HBREQ0#	E7	H_BREQ#0
HCPURST#	H10	H_CPURST#
HCLKINN	AB1	CLK_MCH_BCLK# 21
HCLKINP	AB2	CLK_MCH_BCLK 21
HDBSY#	C6	H_DBSY#
HDEFER#	E6	H_DEFER#
HDINV0#	H8	H_DINV#0
HDINV1#	K3	H_DINV#1
HDINV2#	T7	H_DINV#2
HDINV3#	U5	H_DINV#3
HDPWR#	G6	H_DPWR#
HDRDY#	E7	H_DRDY#
HDSTBN0#	G4	H_DSTBN#0
HDSTBN1#	K1	H_DSTBN#1
HDSTBN2#	R3	H_DSTBN#2
HDSTBN3#	V3	H_DSTBN#3
HDSTBP0#	G5	H_DSTBP#0
HDSTBP1#	K2	H_DSTBP#1
HDSTBP2#	R2	H_DSTBP#2
HDSTBP3#	W4	H_DSTBP#3
HEDRDY#	F6	TP_H_EDRDY#
HHIT#	D4	H_HIT#
HHITM#	D6	H_HITM#
HLOCK#	B3	TP_H_PCREQ#
HPCREQ#	A11	TP_H_PCREQ#
HREQ0#	A7	H_REQ#0
HREQ1#	D7	H_REQ#1
HREQ2#	B8	H_REQ#2
HREQ3#	C7	H_REQ#3
HREQ4#	A8	H_REQ#4
HRS0#	A4	H_RS#0
HRS1#	C5	H_RS#1
HRS2#	B4	H_RS#2
HCPUSLP#	G8	H_CPUSLP#
HTRDY#	B5	H_TRDY#

H_A#[31..3] 3



TPC28t 1 OT223

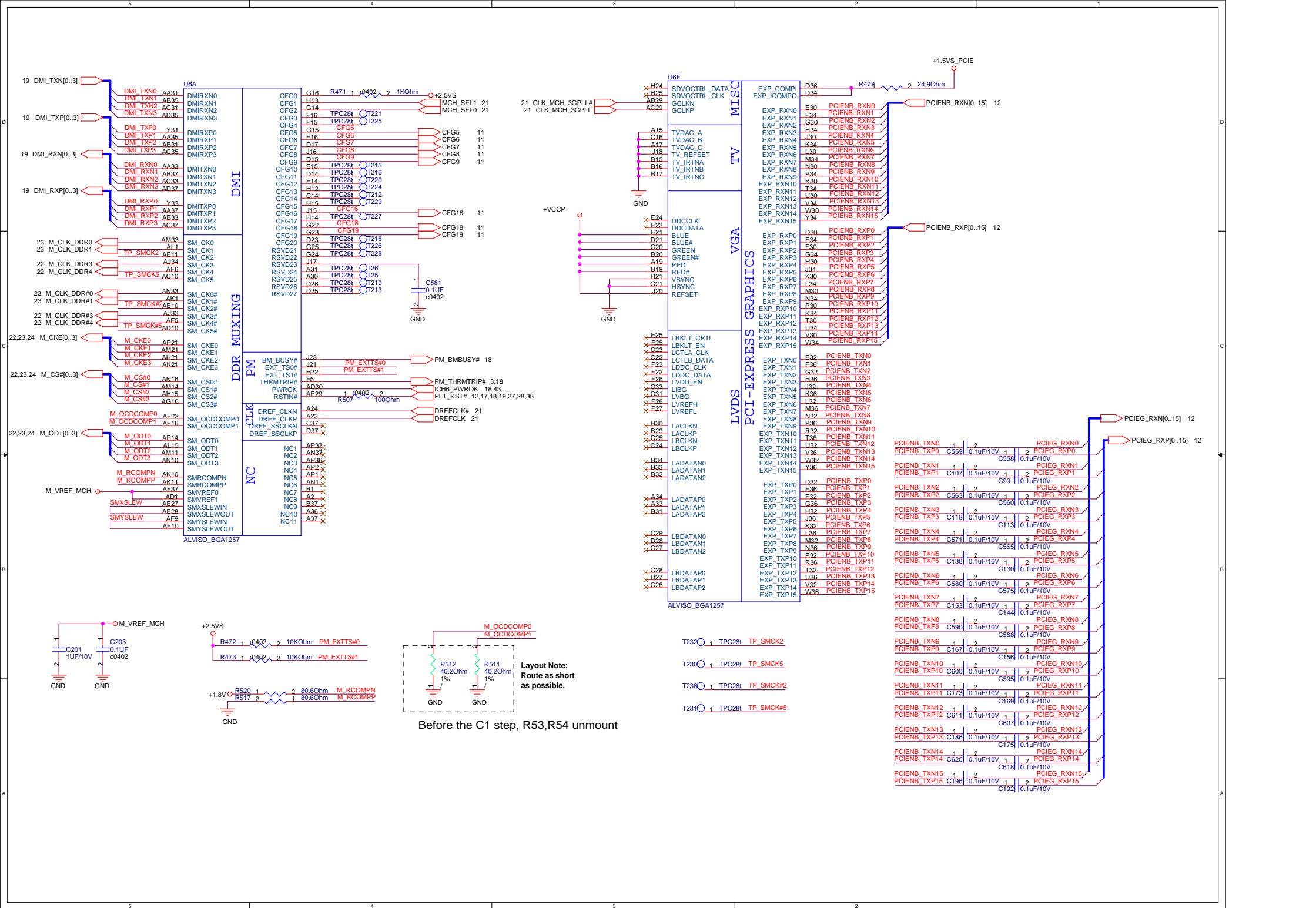
H_LOCK# 3

H_REQ#[4..0] 3

H_RS#[0..2] 3

H_CPUSLP# 3,18

H_TRDY# 3



23 M_A_DQ[0..63]

U6B

DDR SYSTEM MEMORY A

M_A_DQ0 AG35
M_A_DQ1 AH35
M_A_DQ2 AL35
M_A_DQ3 AH36
M_A_DQ4 AJ35
M_A_DQ5 AK37
M_A_DQ6 AL34
M_A_DQ7 AM36
M_A_DQ8 AL34
M_A_DQ9 AM35
M_A_DQ10 AP32
M_A_DQ11 AM31
M_A_DQ12 AM34
M_A_DQ13 AM35
M_A_DQ14 AL32
M_A_DQ15 AM32
M_A_DQ16 AN31
M_A_DQ17 AP31
M_A_DQ18 AN28
M_A_DQ19 AP28
M_A_DQ20 AL30
M_A_DQ21 AM30
M_A_DQ22 AM28
M_A_DQ23 AL28
M_A_DQ24 AP27
M_A_DQ25 AM27
M_A_DQ26 AM23
M_A_DQ27 AM22
M_A_DQ28 AL23
M_A_DQ29 AM24
M_A_DQ30 AN22
M_A_DQ31 AP22
M_A_DQ32 AM9
M_A_DQ33 AL9
M_A_DQ34 AL6
M_A_DQ35 AP7
M_A_DQ36 AP11
M_A_DQ37 AP10
M_A_DQ38 AL7
M_A_DQ39 AM7
M_A_DQ40 AN5
M_A_DQ41 AN6
M_A_DQ42 AN3
M_A_DQ43 AP3
M_A_DQ44 AP6
M_A_DQ45 AM6
M_A_DQ46 AL4
M_A_DQ47 AM3
M_A_DQ48 AK2
M_A_DQ49 AK3
M_A_DQ50 AG2
M_A_DQ51 AG1
M_A_DQ52 AL3
M_A_DQ53 AM2
M_A_DQ54 AH3
M_A_DQ55 AG3
M_A_DQ56 AF3
M_A_DQ57 AE3
M_A_DQ58 AD6
M_A_DQ59 AF4
M_A_DQ60 AF2
M_A_DQ61 AF1
M_A_DQ62 AD4
M_A_DQ63 AD5

SA_BS0#
SA_BS1#
SA_BS2#
SA_DM0
SA_DM1
SA_DM2
SA_DM3
SA_DM4
SA_DM5
SA_DM6
SA_DM7

AK15
AK16
AL21
AJ37
AP35
AL29
AP24
AP9
AP4
AJ2
AD3

M_A_BS#0 23,24
M_A_BS#1 23,24
M_A_BS#2 23,24
M_A_DM[0..7] 23

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

AK36
AP33
AN29
AP23
AM8
AM4
AJ1
AE5

M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7

AK35
AP34
AN30
AN23
AM6
AM5
AH1
AE4

M_A_A[0..13] 23,24

AL17
AP17
AP18
AM17
AN18
AM18
AL19
AP20
AM19
AL20
AM16
AN20
AM20
AM15

M_A_CAS# 23,24
M_A_RAS# 23,24
M_A_WE# 23,24

AN15
AP16
AF29
AF28
AP15

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22 M_B_DQ[0..63]

U6C

DDR SYSTEM MEMORY B

M_B_DQ0 AE31
M_B_DQ1 AE32
M_B_DQ2 AG32
M_B_DQ3 AG36
M_B_DQ4 AE34
M_B_DQ5 AE33
M_B_DQ6 AF31
M_B_DQ7 AF30
M_B_DQ8 AH33
M_B_DQ9 AH32
M_B_DQ10 AK31
M_B_DQ11 AG30
M_B_DQ12 AG34
M_B_DQ13 AG33
M_B_DQ14 AH31
M_B_DQ15 AJ31
M_B_DQ16 AK30
M_B_DQ17 AJ30
M_B_DQ18 AH29
M_B_DQ19 AH28
M_B_DQ20 AK29
M_B_DQ21 AH30
M_B_DQ22 AH27
M_B_DQ23 AG28
M_B_DQ24 AF24
M_B_DQ25 AG23
M_B_DQ26 AJ22
M_B_DQ27 AK22
M_B_DQ28 AH24
M_B_DQ29 AH23
M_B_DQ30 AG22
M_B_DQ31 AJ21
M_B_DQ32 AG10
M_B_DQ33 AG9
M_B_DQ34 AG8
M_B_DQ35 AH8
M_B_DQ36 AH11
M_B_DQ37 AH10
M_B_DQ38 AJ9
M_B_DQ39 AK9
M_B_DQ40 AJ7
M_B_DQ41 AK6
M_B_DQ42 AJ4
M_B_DQ43 AH5
M_B_DQ44 AK8
M_B_DQ45 AJ8
M_B_DQ46 AJ5
M_B_DQ47 AK4
M_B_DQ48 AG5
M_B_DQ49 AG4
M_B_DQ50 AD8
M_B_DQ51 AD9
M_B_DQ52 AH4
M_B_DQ53 AE8
M_B_DQ54 AG6
M_B_DQ55 AD7
M_B_DQ56 AC5
M_B_DQ57 AB8
M_B_DQ58 AB6
M_B_DQ59 AB5
M_B_DQ60 AC8
M_B_DQ61 AC7
M_B_DQ62 AA4
M_B_DQ63 AA5

SB_BS0#
SB_BS1#
SB_BS2#
SB_DM0
SB_DM1
SB_DM2
SB_DM3
SB_DM4
SB_DM5
SB_DM6
SB_DM7

AJ15
AG17
AG21
AF32
AK27
AK24
AJ10
AK5
AE7
AB7

M_B_BS#0 22,24
M_B_BS#1 22,24
M_B_BS#2 22,24
M_B_DM[0..7] 22

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

AF34
AK32
AJ28
AK23
AM10
AH6
AF8
AB4

M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7

AF35
AK33
AK28
AJ23
AL10
AH7
AF7
AB5

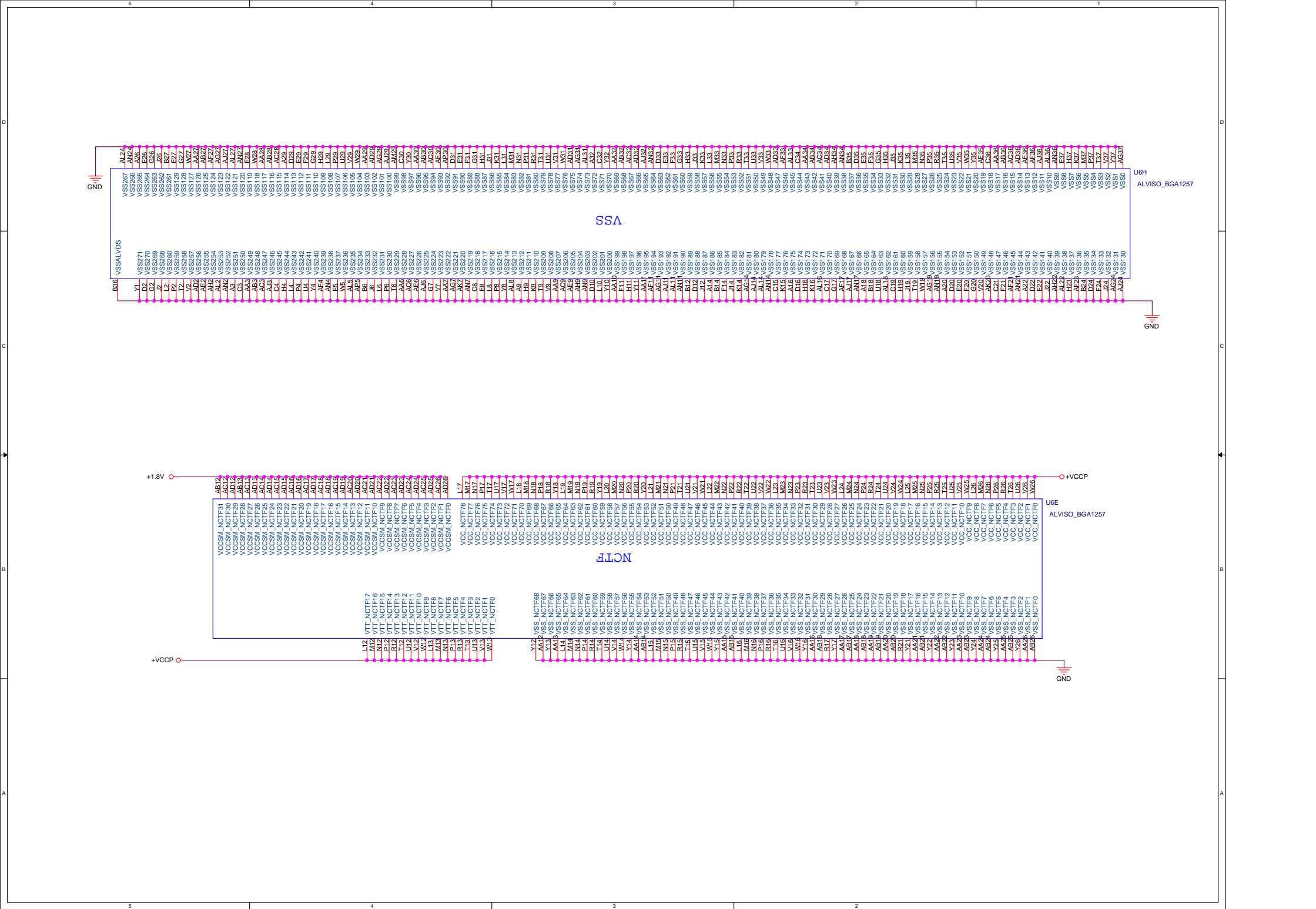
M_B_A[0..13] 22,24

AH17
AK17
AH18
AJ18
AK18
AJ19
AH19
AJ20
AH20
AJ16
AG18
AG20
AG15

M_B_CAS# 22,24
M_B_RAS# 22,24
M_B_WE# 22,24

AH14
AK14
AF15
AF14
AH16

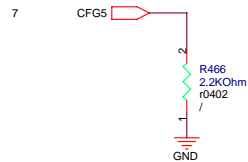
ALVISO_BGA1257



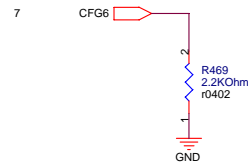
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
LOW = No SDVO
device present
(Default)

CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)

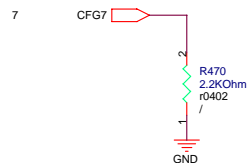


CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)



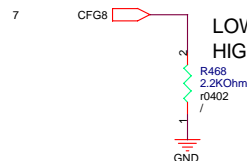
CFG7 : CPU STRAP

LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



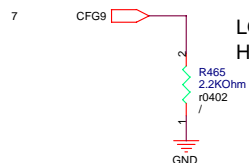
CFG8 : PCI-X POWER Saving

LOW = PCI-X POWER Saving
HIGH (Default)



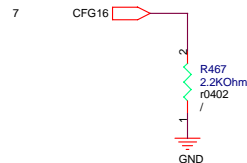
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



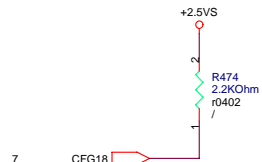
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



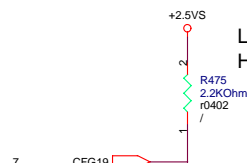
CFG18 : VCC SELECT

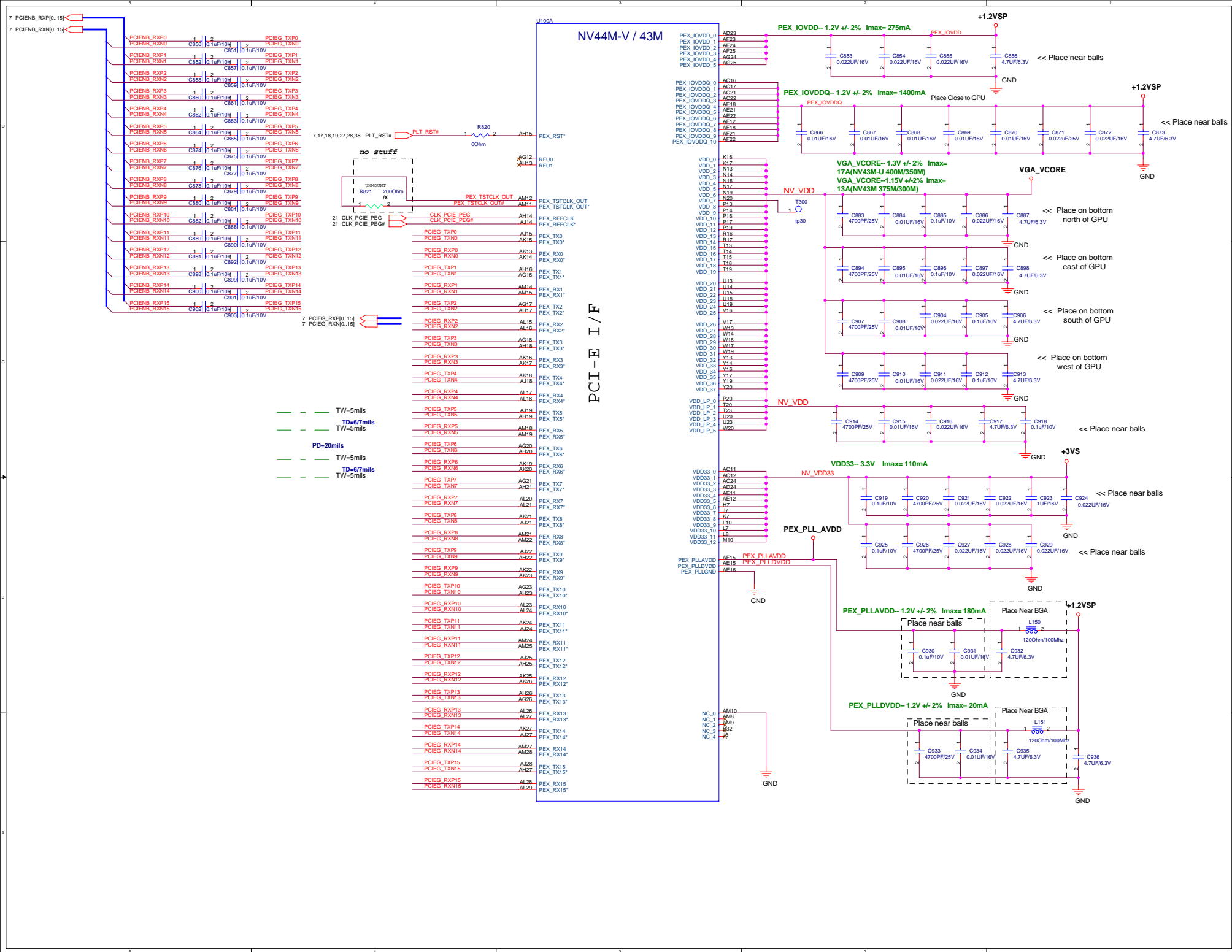
LOW = 1.05V (Default)
HIGH = 1.5V



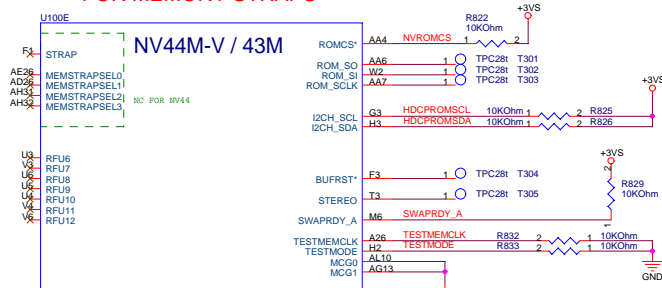
CFG19 : VTT SELECT

LOW = 1.05V (Default)
HIGH = 1.2V

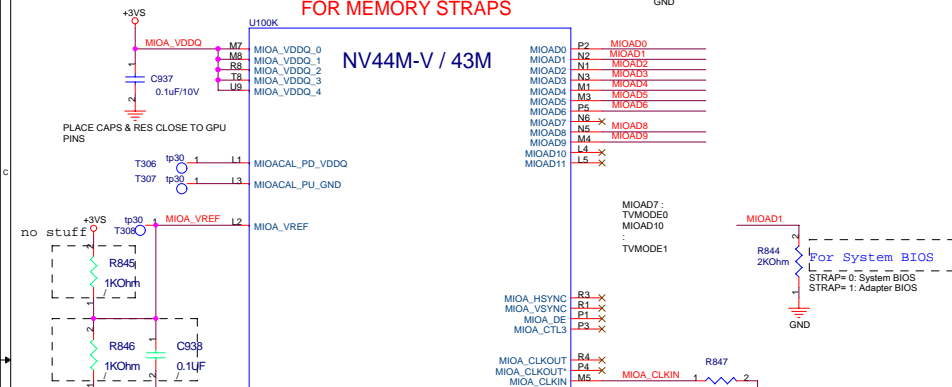




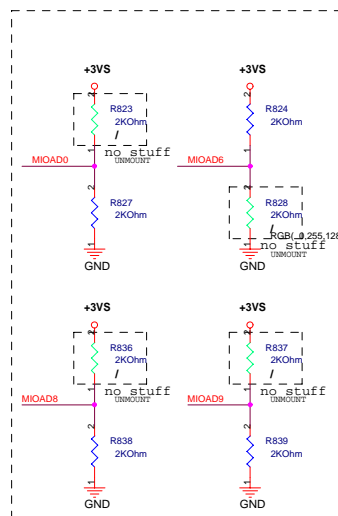
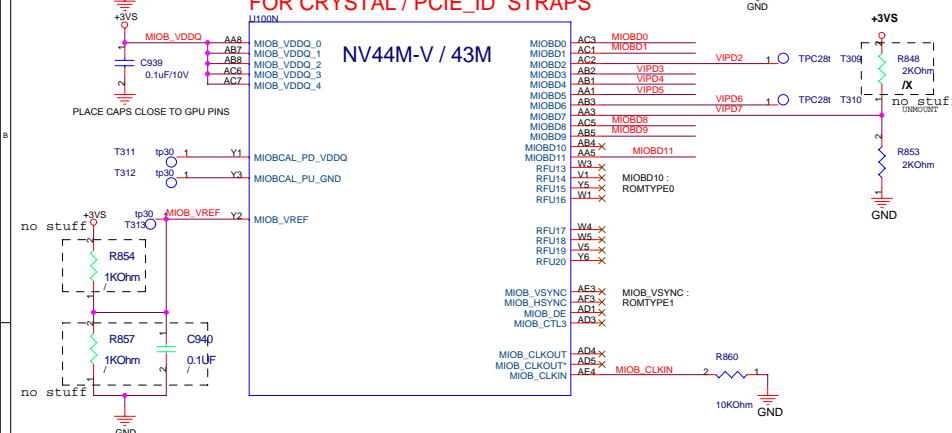
FOR MEMORY STRAPS



FOR MEMORY STRAPS

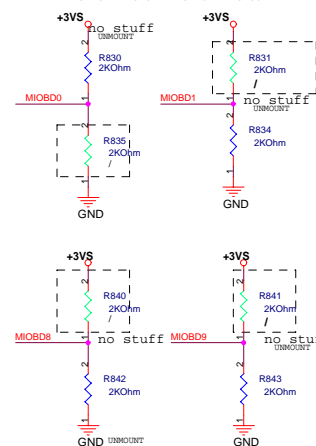


FOR CRYSTAL / PCIE_ID STRAPS



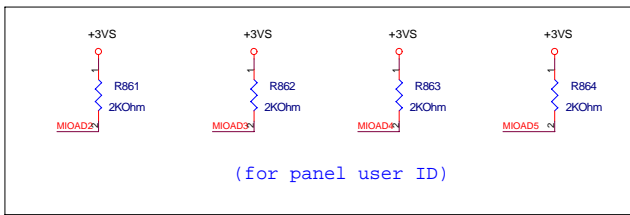
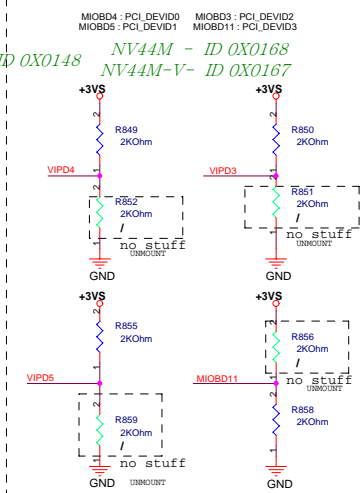
MEM TYPE STRAP

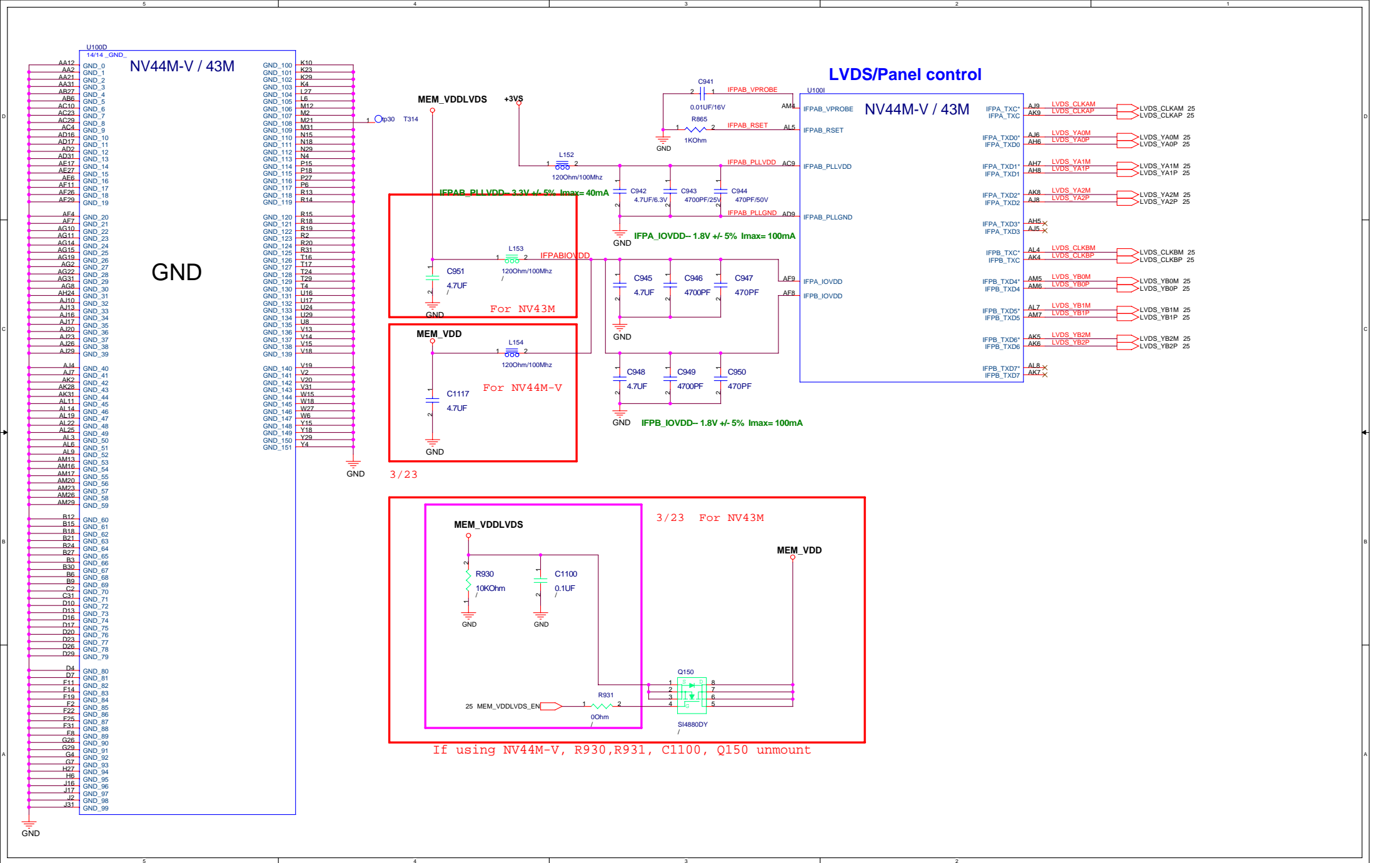
```
NV44M memory strap setting:
01 (0001) SAMSUNG 8MX32X2 64MB (two VRAM) -> 1.8V
01 (0001) HYNIX 8MX32X2 64MB (two VRAM) -> 1.8V
04 (0100) SAMSUNG 4MX32X2 32MB (two VRAM) -> 1.8V
09 (1001) HYNIX 8MX32X1 32MB (one VRAM) -> 1.8V
0C (1100) SAMSUNG 4MX32X1 16MB (one VRAM) ->
1.8V
MIOBD0 : RAMCFG0      MIOBD1 : RAMCFG1
MIOBD8 : RAMCFG2      MIOBD9 : RAMCFG3
```



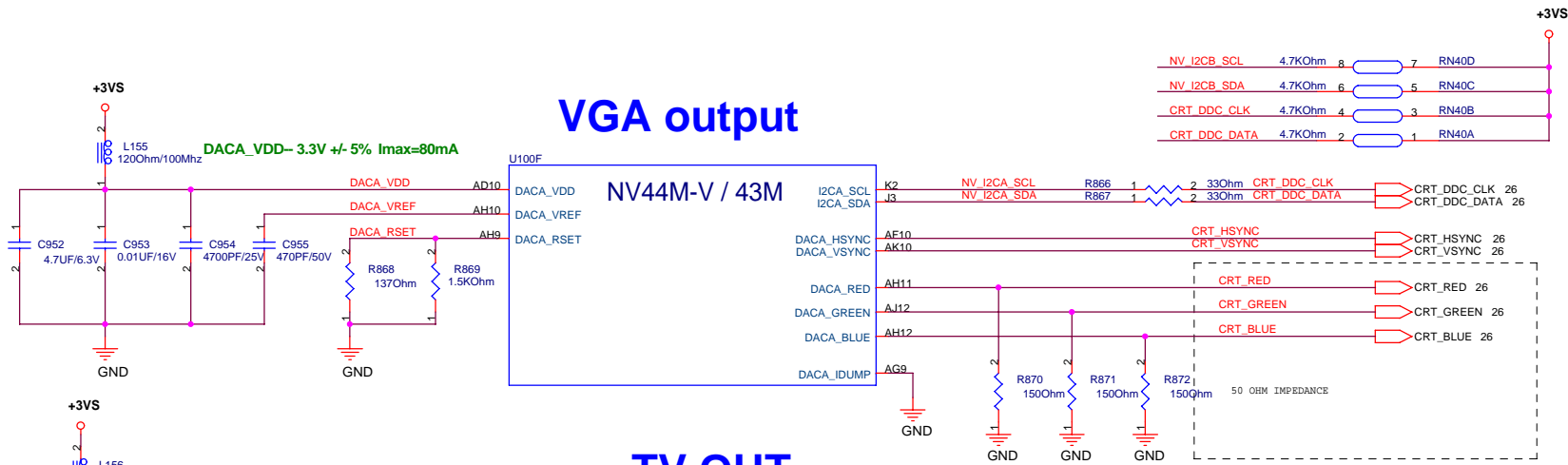
```
(PCI_DEVICE_ID)
```

NV43M - ID 0X0148 *NV44M - ID 0X0168*
NV44M-V- ID 0X0167

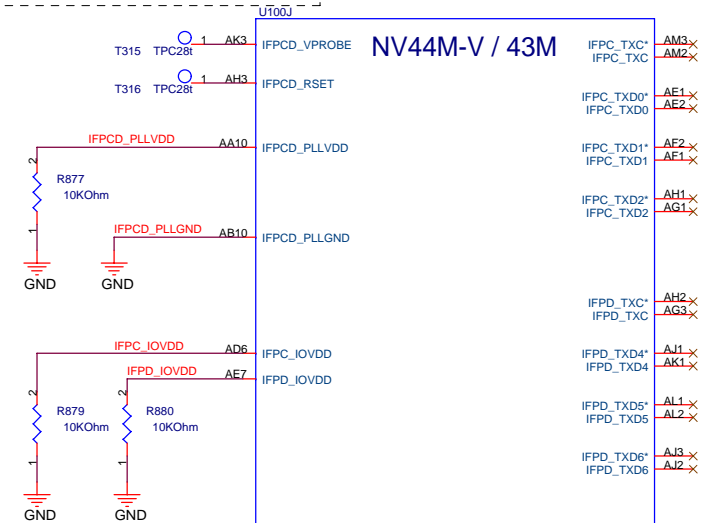
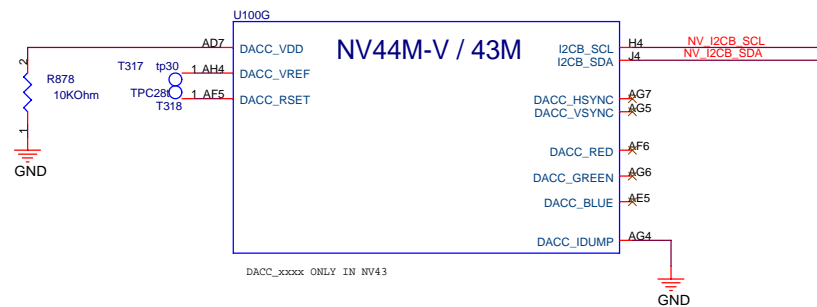
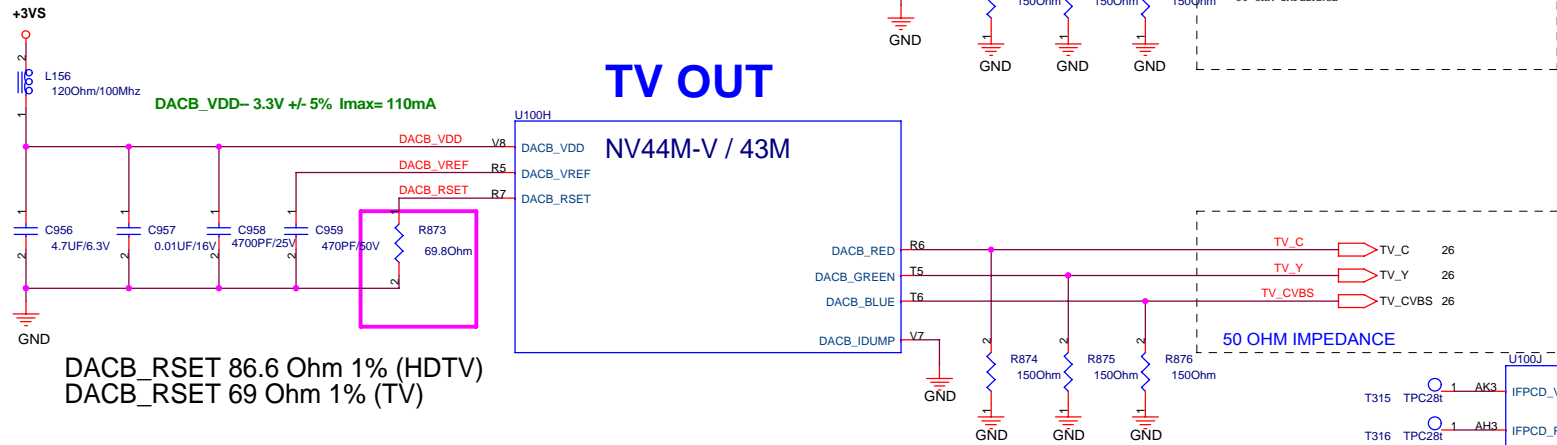




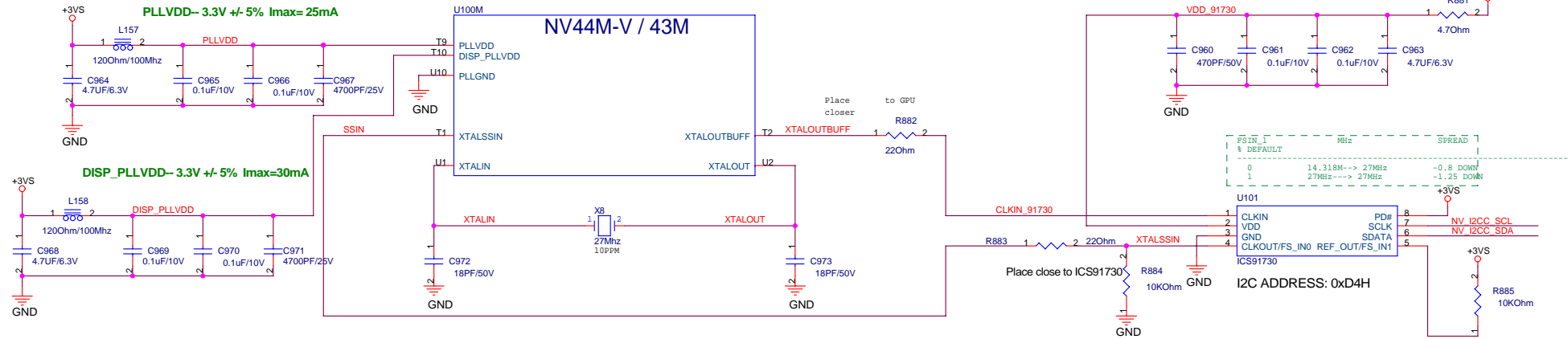
VGA output



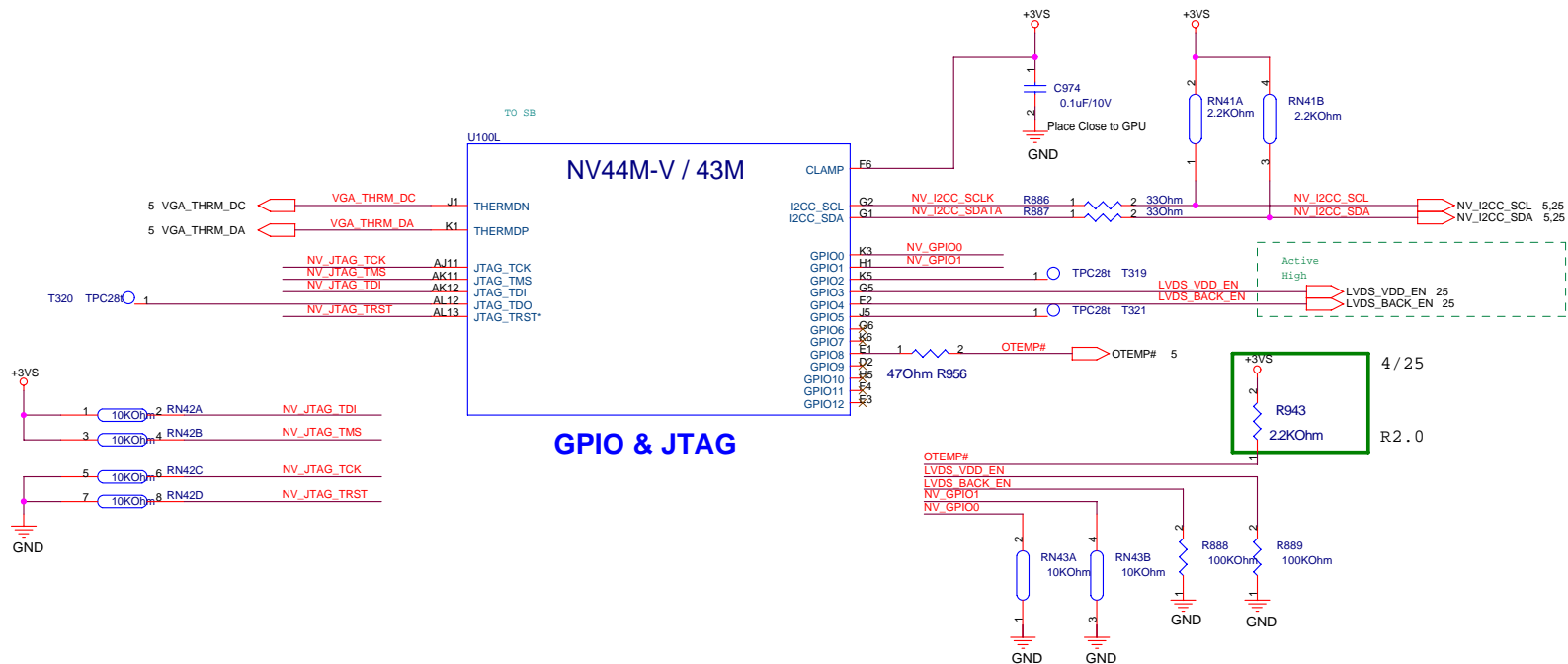
TV OUT



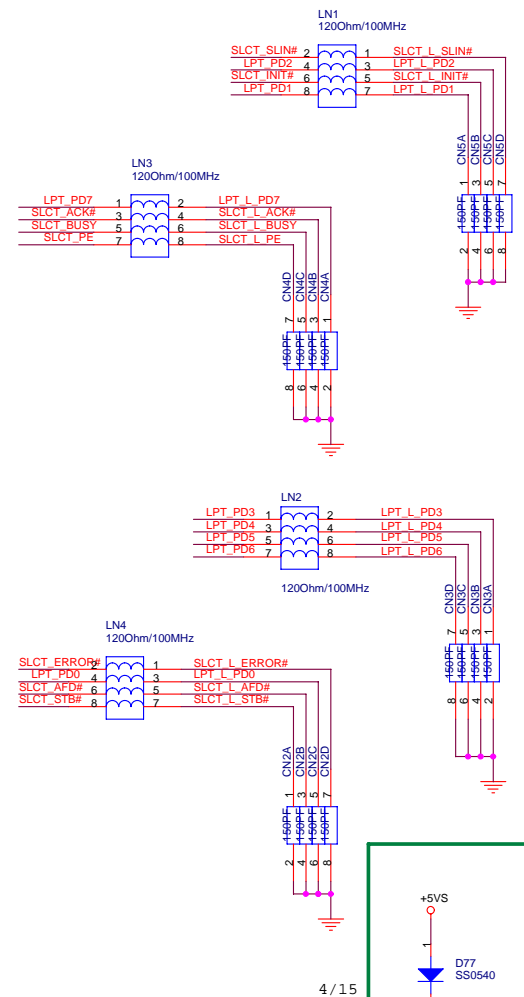
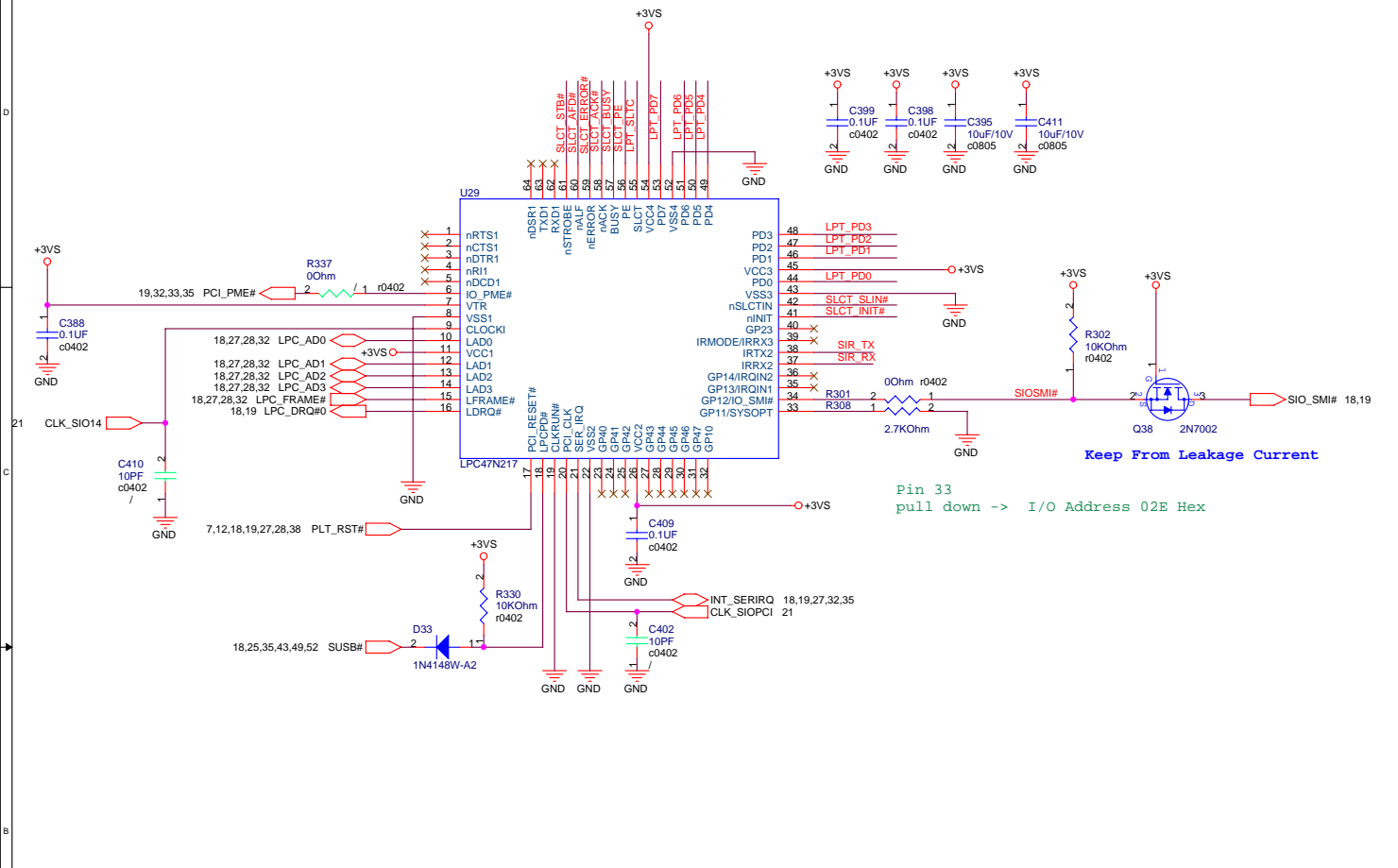
XTAL/PLL/VDD



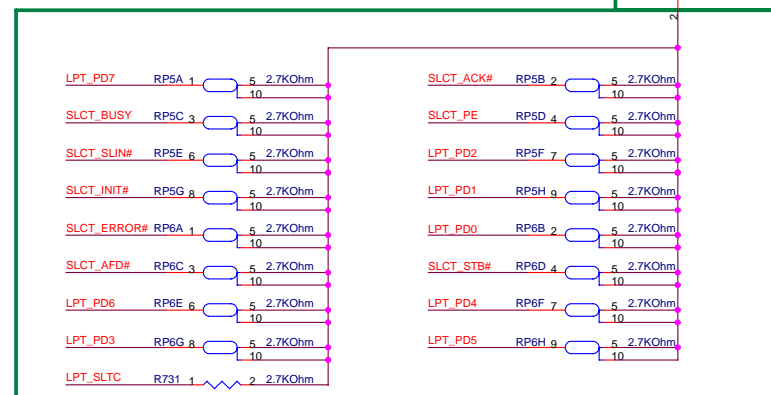
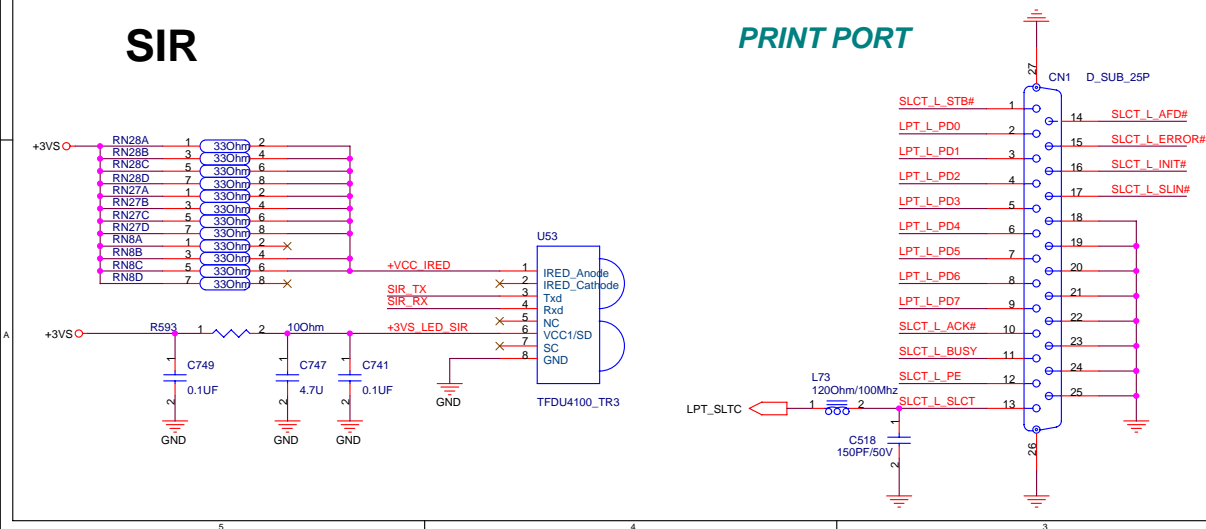
NV44M-V / 43M

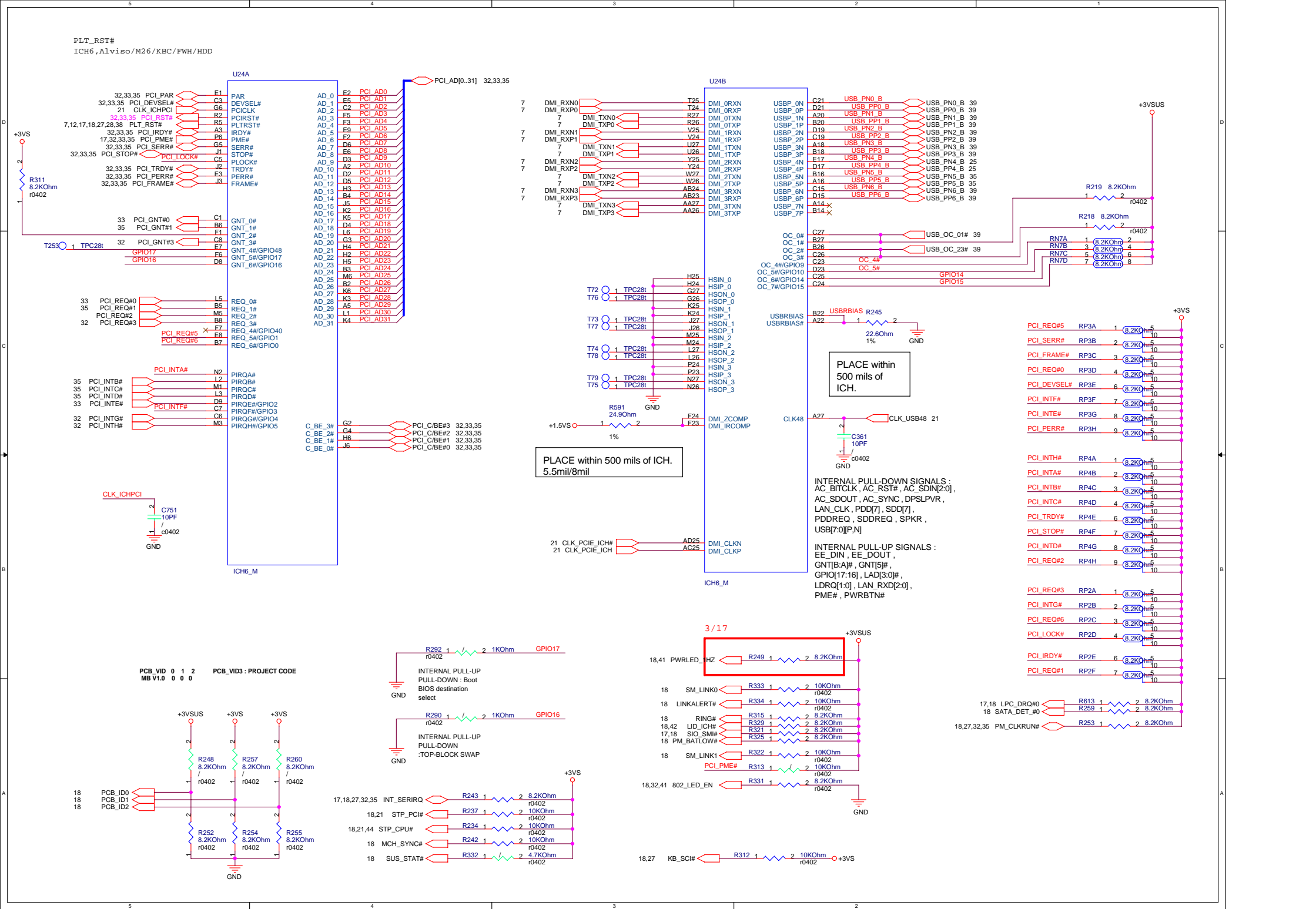


Super I/O

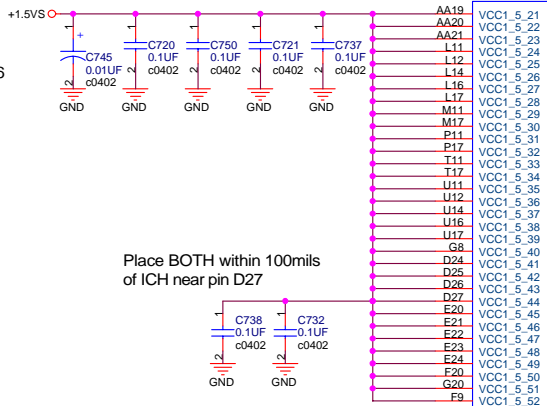


SIR

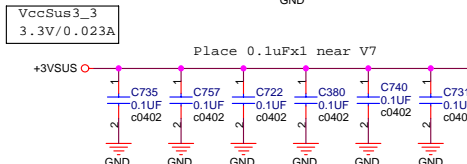
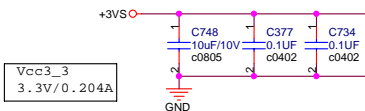
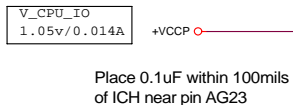




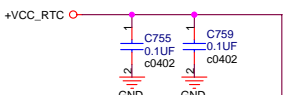
Place 0.01uF within 100mils of ICH
near pin AA19
Place 4X0.1uF Distribute near pin ICH6
Package edge



Place 0.1uF near AG10
Place 0.1uF near E26, E27
Place 0.1uF near AG13, AG16
Place 0.1uF near A2-A6,
D1-H1

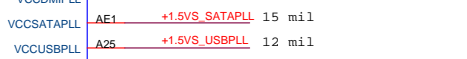
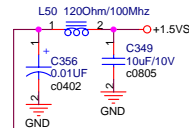
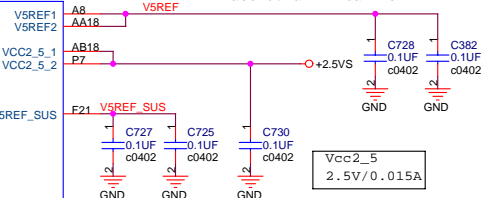


Place BOTH within 100mils of
ICH near pin A17



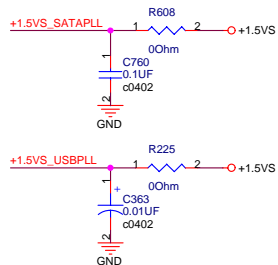
Place 0.1uF near G10

ICH6_M



VCC1_5_B
1.425V/1.5V/1.575V
/ / 578mA

Place 150uF, 3 X 0.1uF within 100mils of
ICH near pin F27, P27, AB27



VCC1_5_A
1.425V/1.5V/1.575V
/ / 1.77A

Place within
100mils of ICH
near pin AG5

Place within
100mils of ICH
near pin AG9

Place 0.1uF near AB18

ICH6_M

ICH6_M

ICH6_M

ICH6_M

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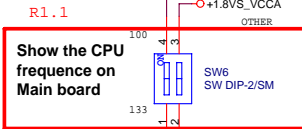
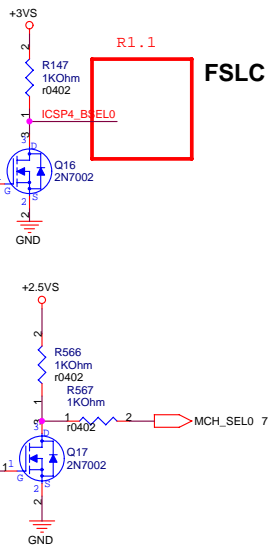
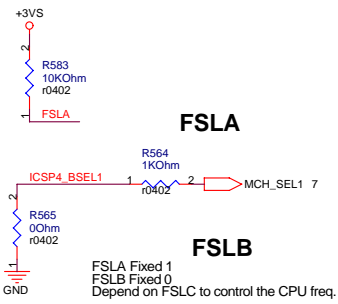
ICH6_M

ICH6_M

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ICH6

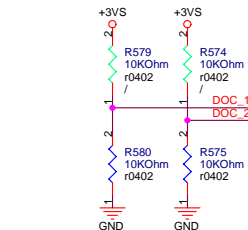
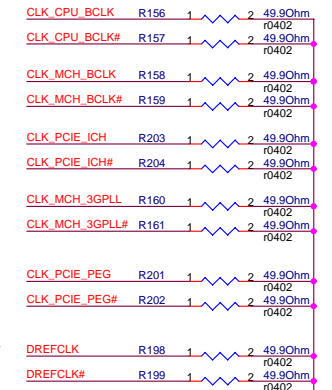


CPU/SW Pins	1	2	3	4
Dothan FSB533	V	V		
Dothan FSB400			V	V

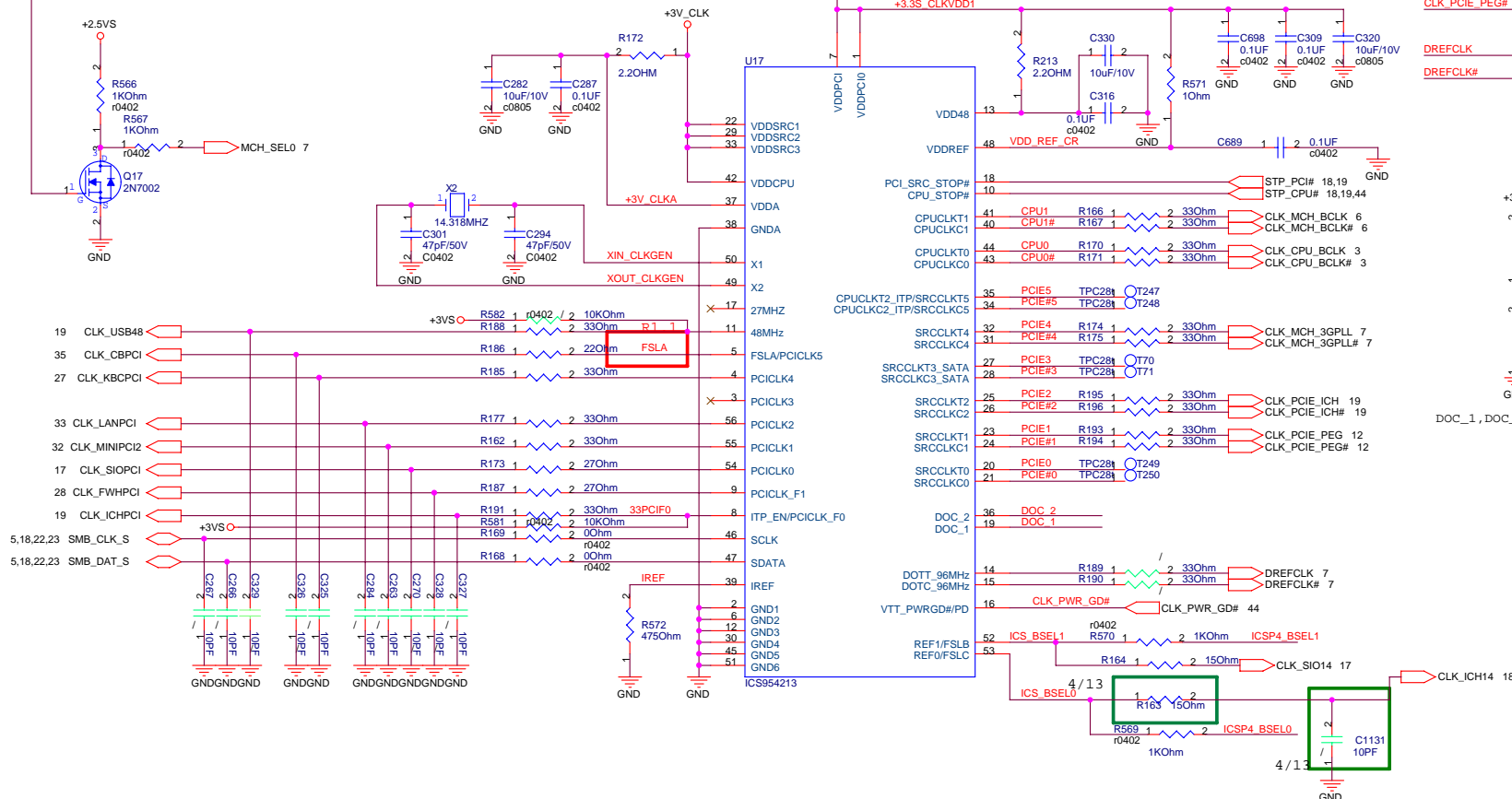
SW1 switch to 1, pin1 & 4 open
SW1 switch to 4, pin1 & 4 short

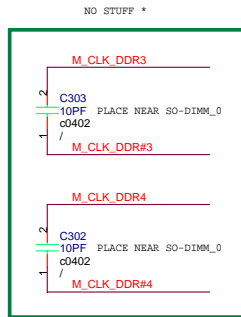
Bit2	Bit1	Bit0	CPU MHz	SRC MHz	SATA MHz	PCI MHz
0	0	0	266.66	100.00	100.00	33.33
0	0	1	133.33	100.00	100.00	33.33
0	1	0	200.00	100.00	100.00	33.33
0	1	1	166.66	100.00	100.00	33.33
1	0	0	333.33	100.00	100.00	33.33
1	0	1	100.00	100.00	100.00	33.33
1	1	0	400.00	100.00	100.00	33.33
1	1	1	0	0	0	0

PLACE termination close to source IC

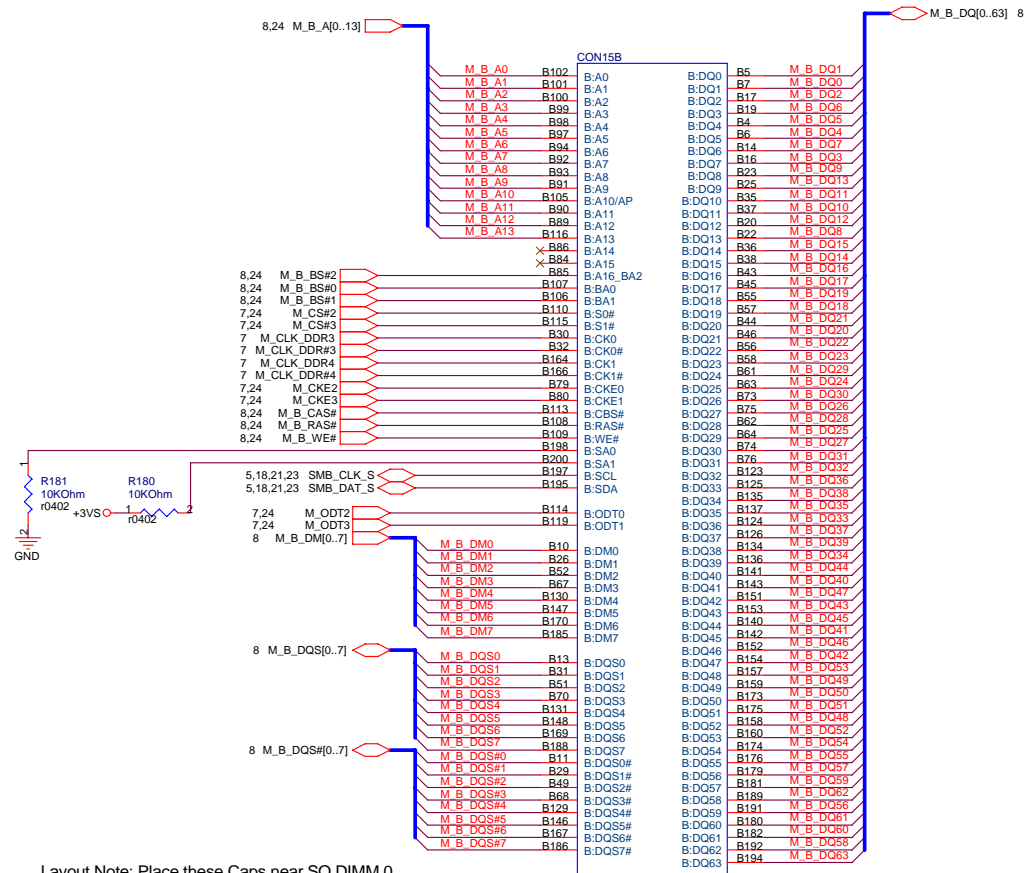


DOC_1, DOC_2 -> L:Normal
H:Freq will jump to a preprogrammed value in the I2C

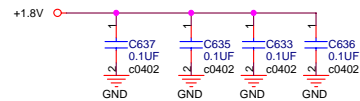




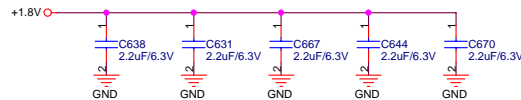
4/13



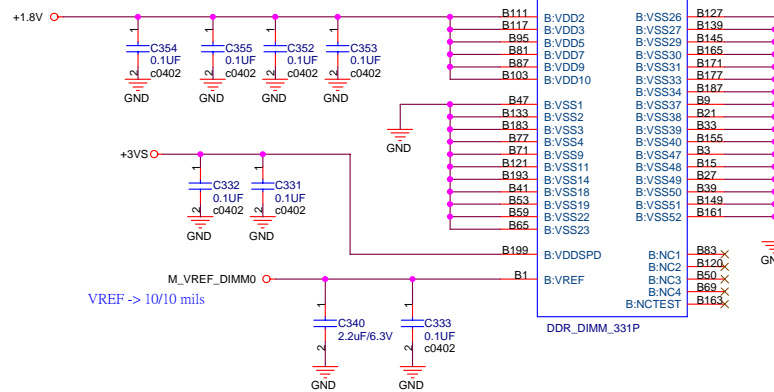
Layout Note: Place these High-Freq decoupling Caps near the GMCH



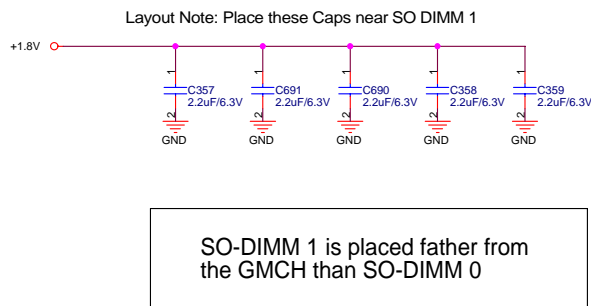
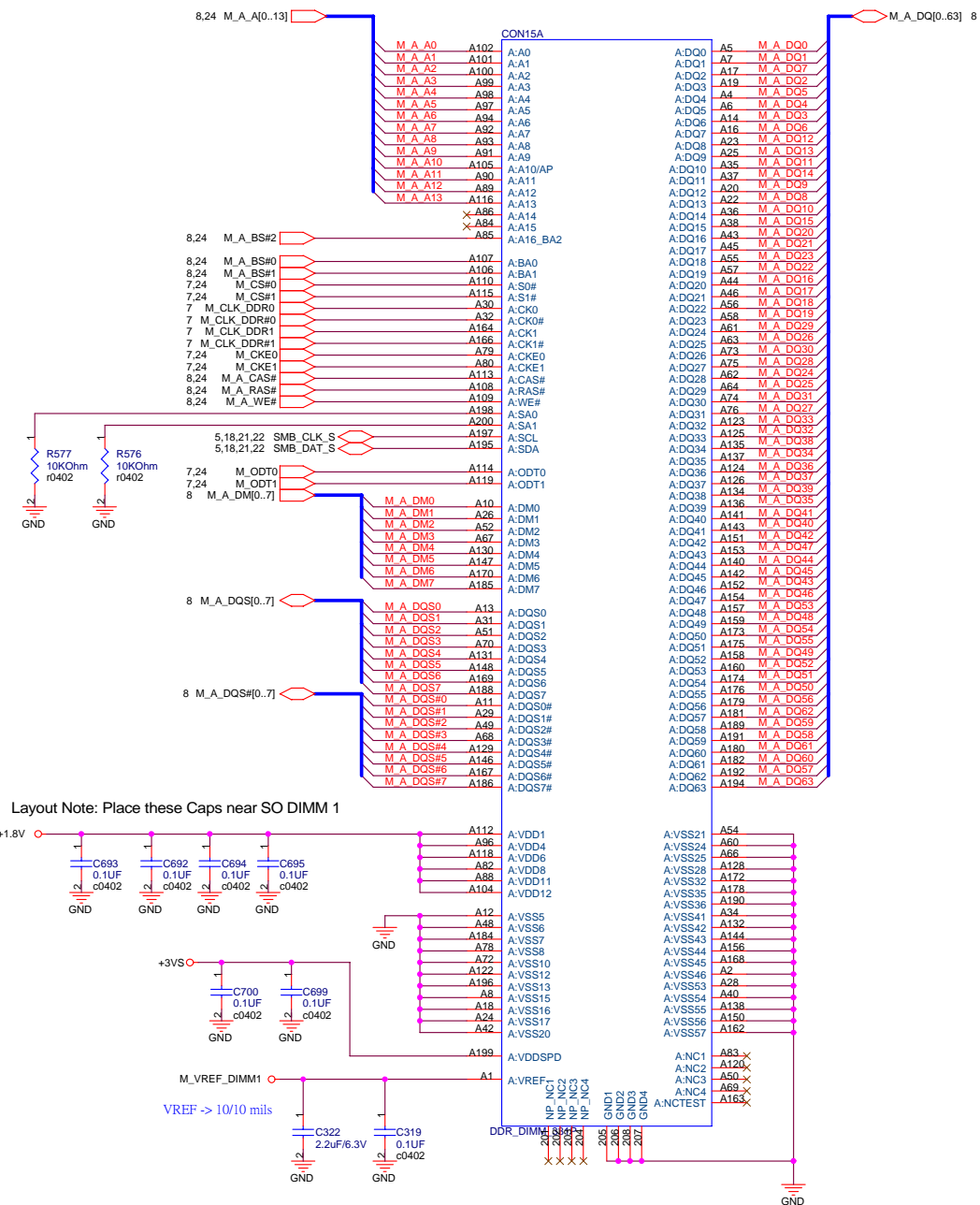
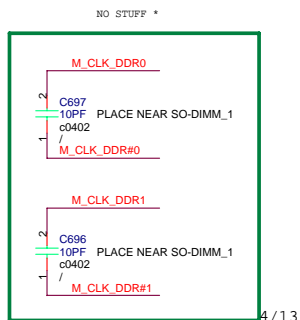
Layout Note: Place these resistors near the GMCH

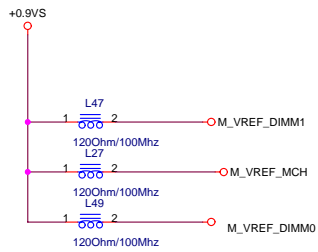


Layout Note: Place these Caps near SO DIMM 0



Layout Note: Place these Caps near SO DIMM 0



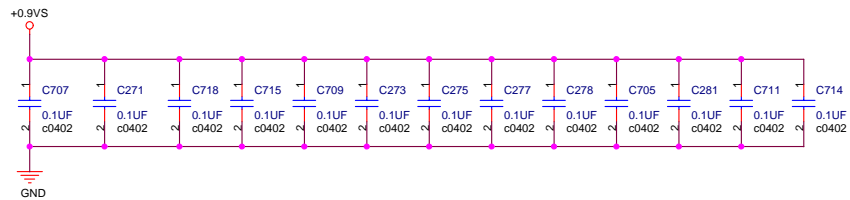


M_A_A[0..13] 8,23
M_A_BS#[0..2] 8,23

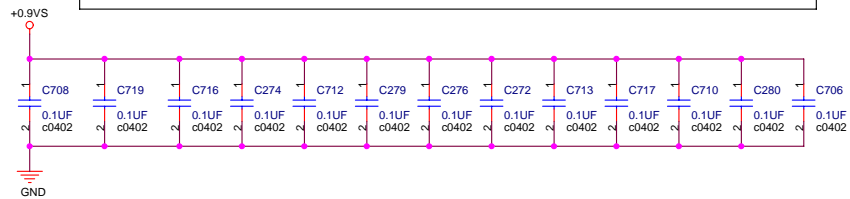
M_A_CAS# 8,23
M_A_RAS# 8,23
M_A_WE# 8,23

M_B_A[0..13] 8,22
M_B_BS#[0..2] 8,22

M_B_CAS# 8,22
M_B_RAS# 8,22
M_B_WE# 8,22



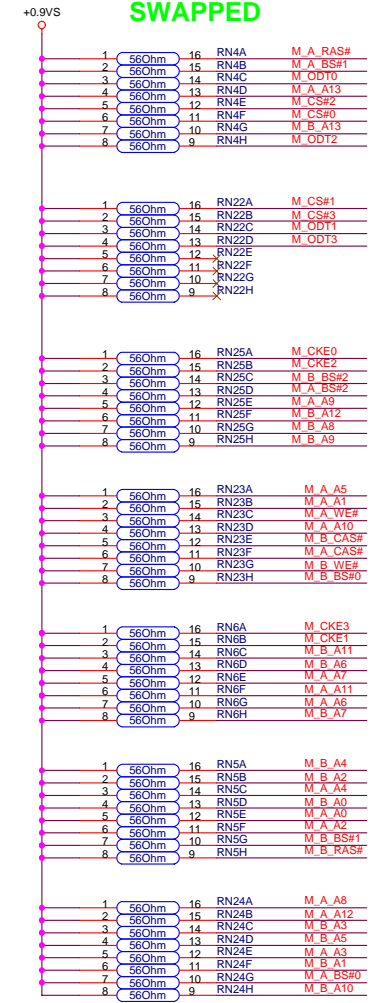
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

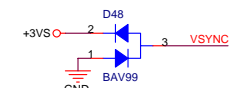
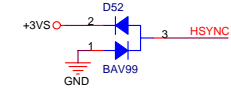
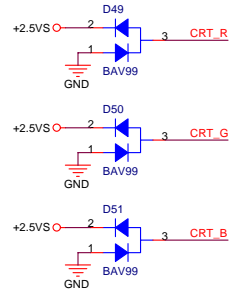


M_CS#[0..3] 7,22,23

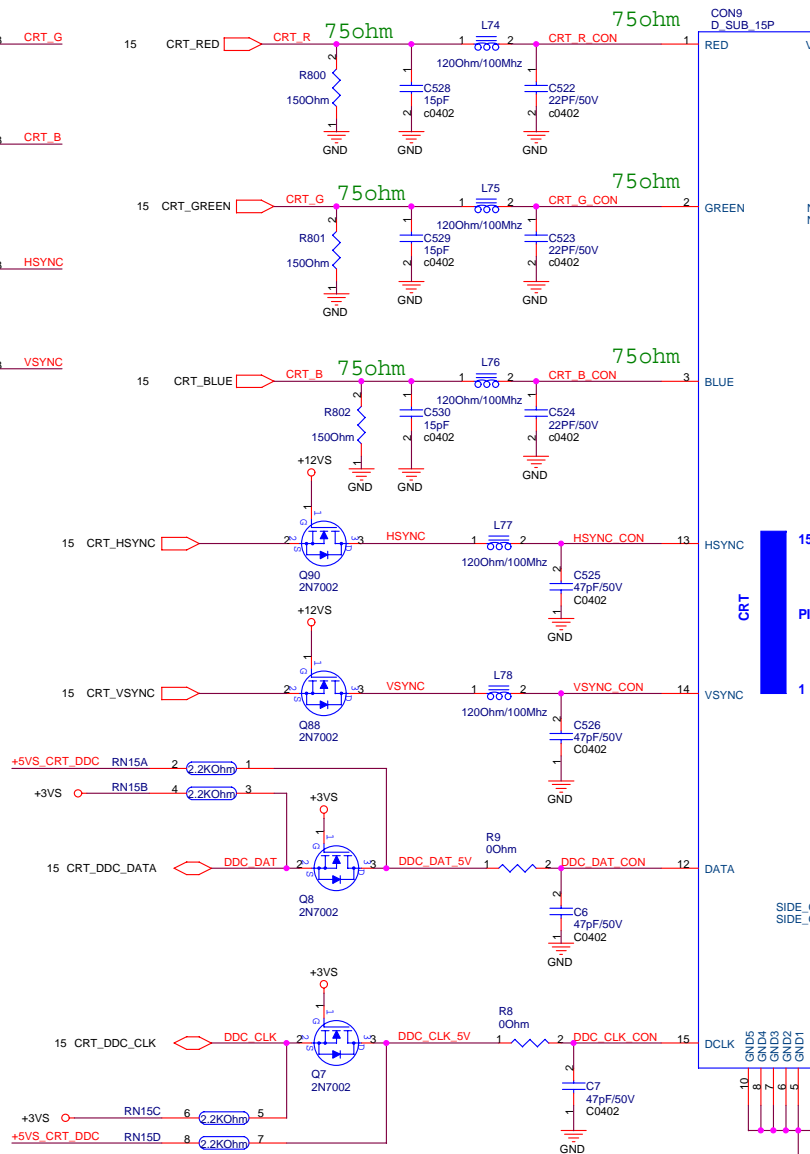
M_ODT[0..3] 7,22,23

M_CKE[0..3] 7,22,23





PLACE ESD
Diodes near
VGA port



50 Ohm

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

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TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

TV_C

TV_CVBS

TV_Y

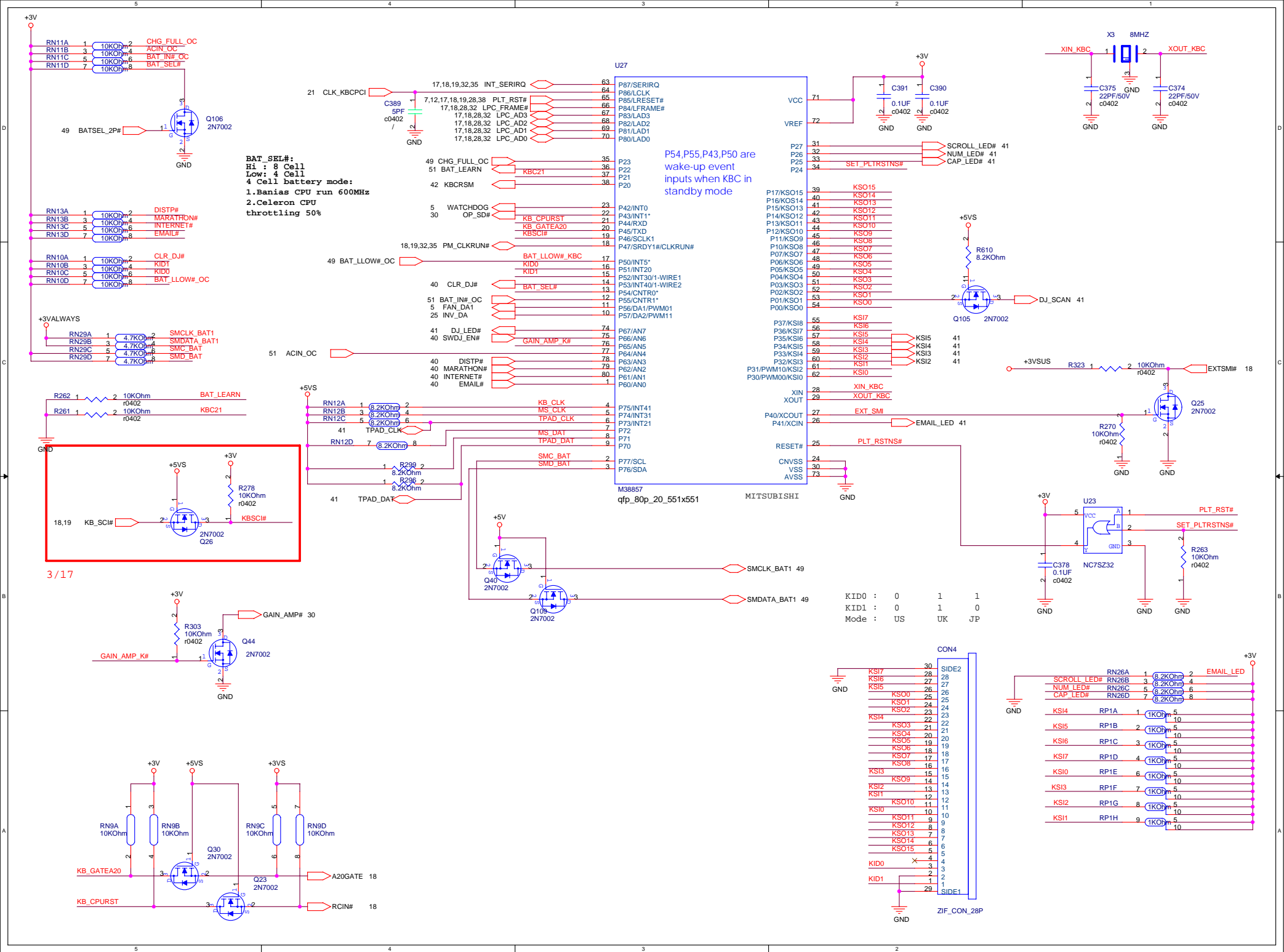
TV_C

TV_CVBS

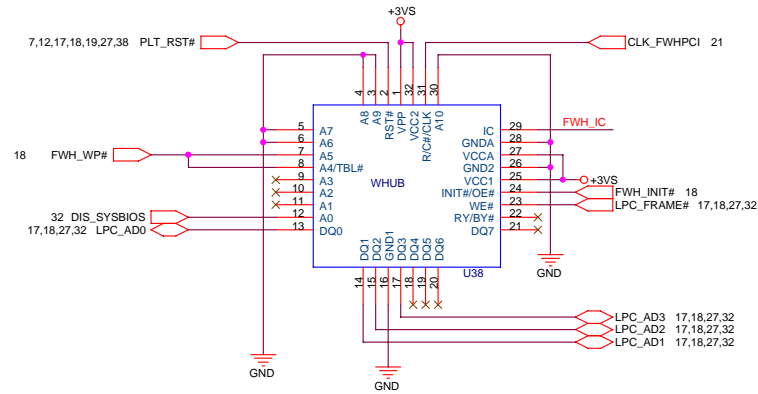
TV_Y

TV_C

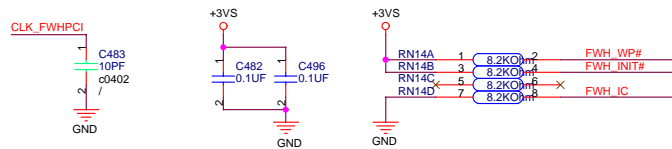
TV_CVBS

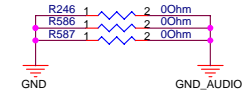
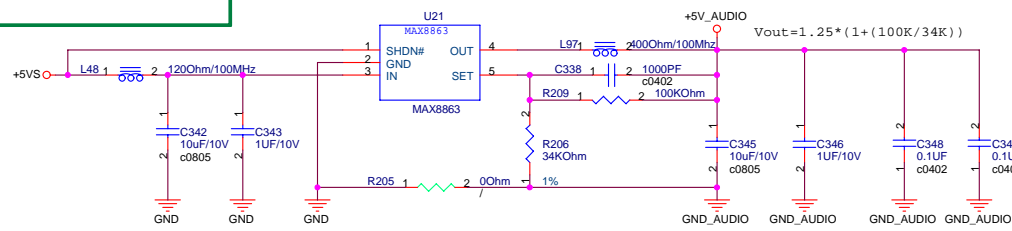
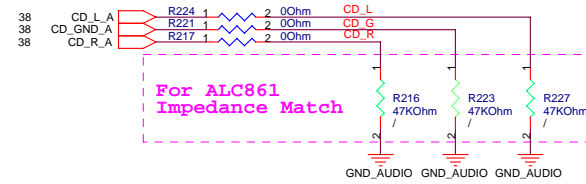
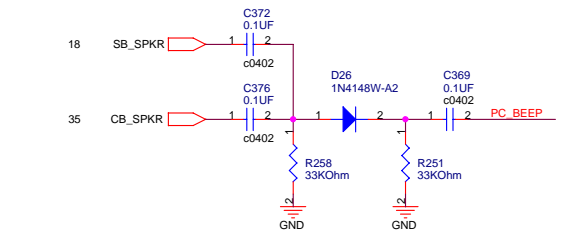
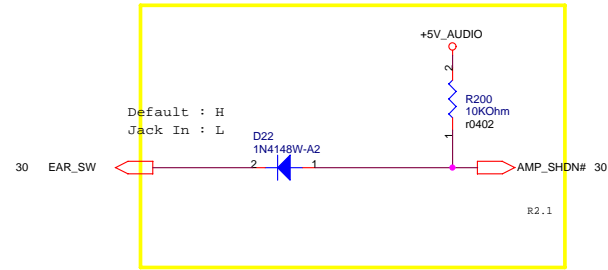
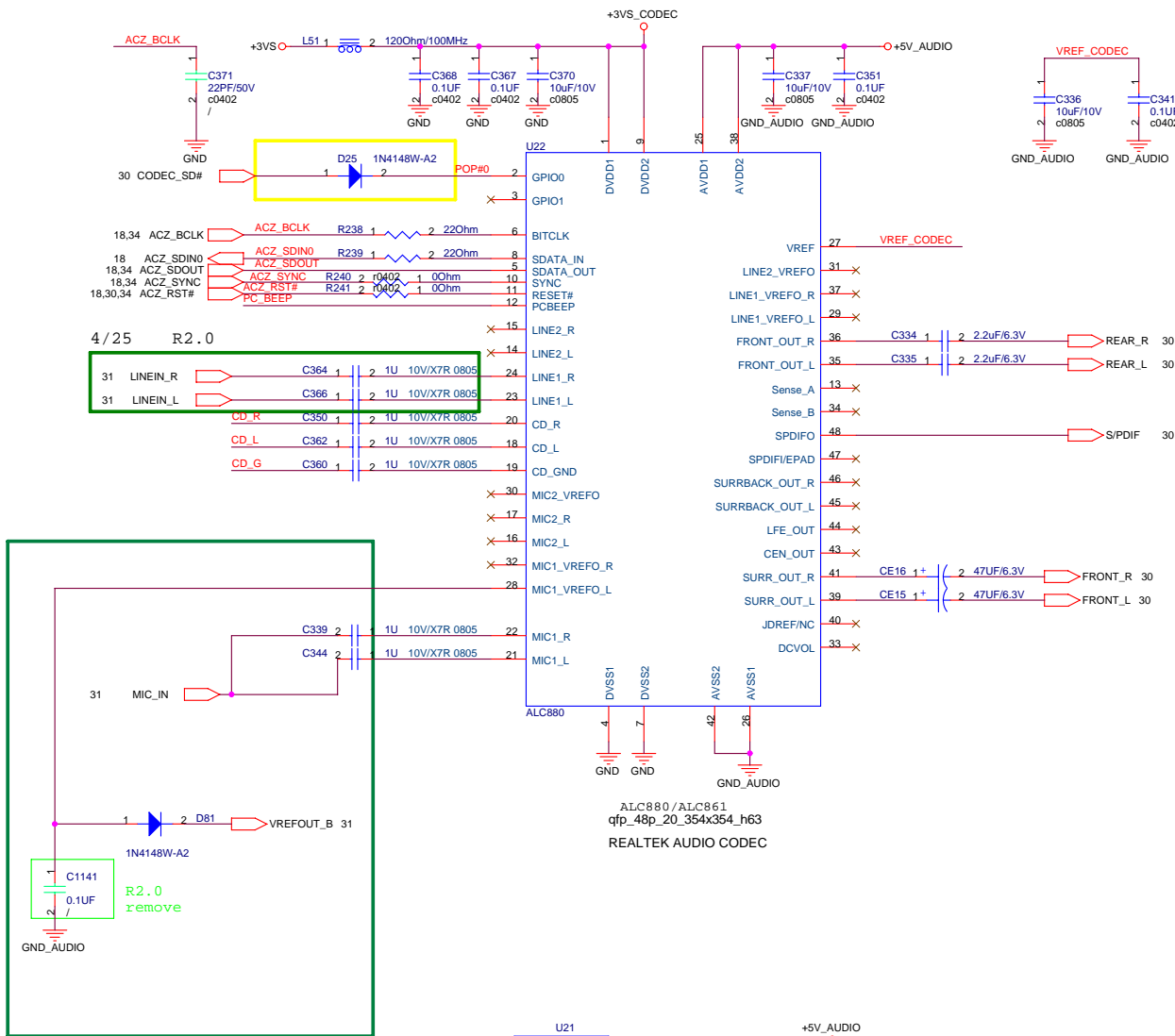


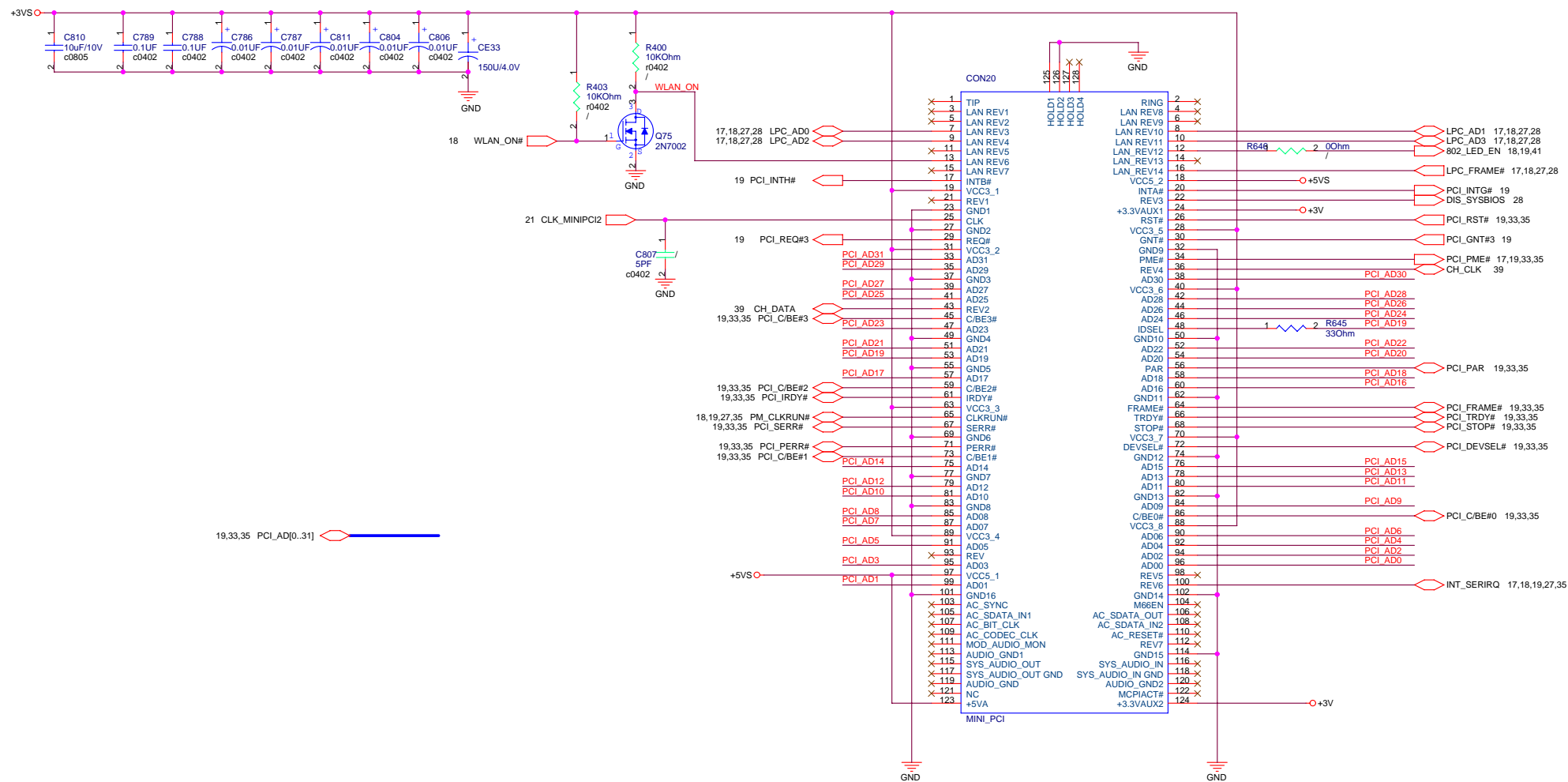
FWH

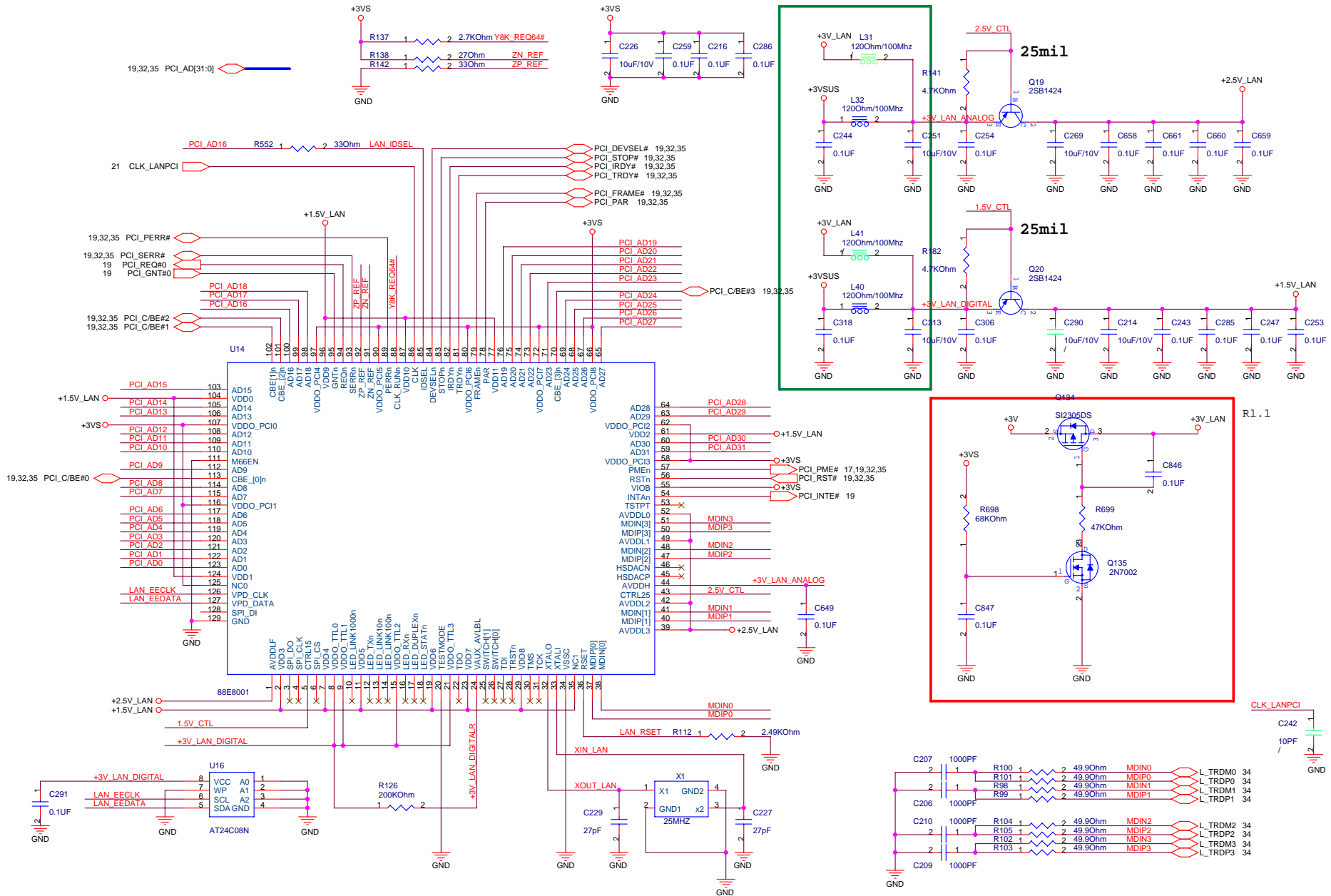


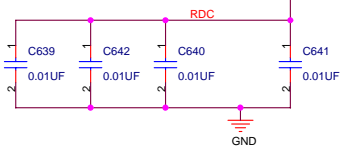
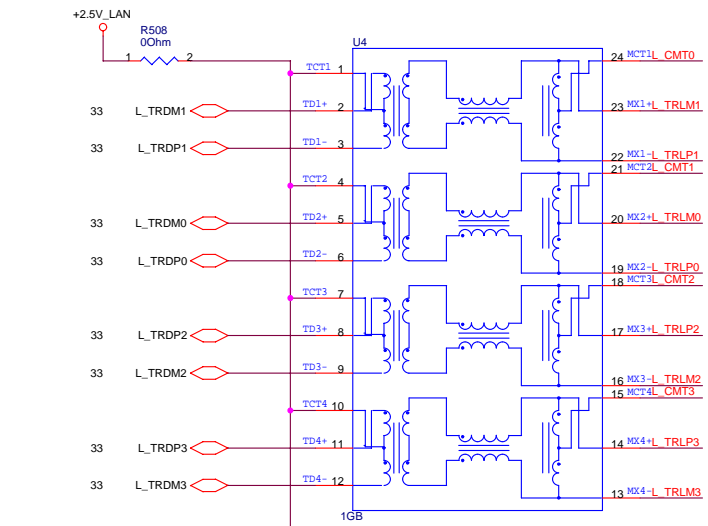
PLCC32 Socket Part Number :
12-043000321
SST FWH/LPC Part Number :
05-001017122(獨)



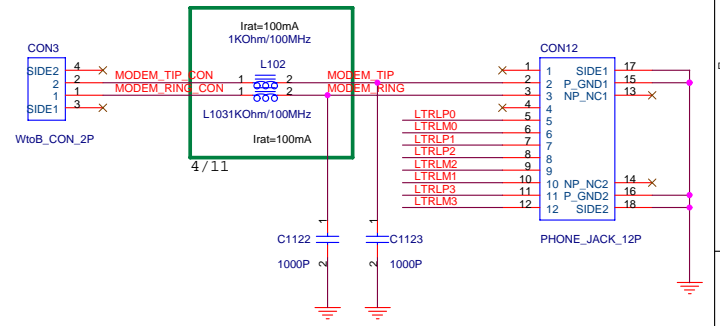
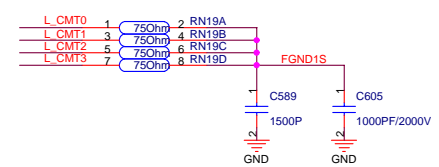
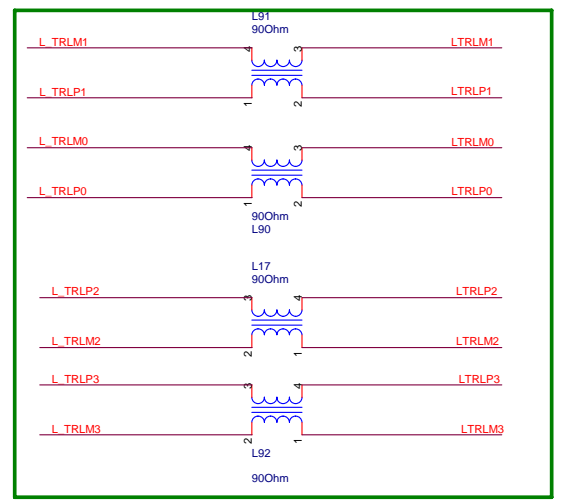




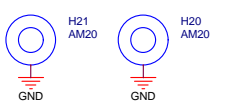
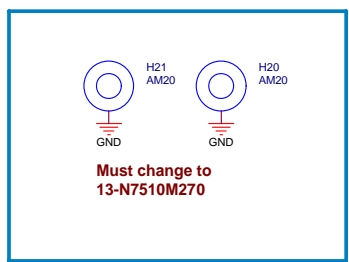
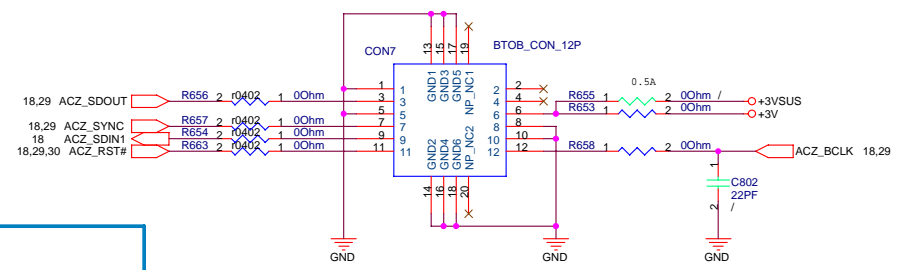
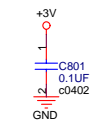




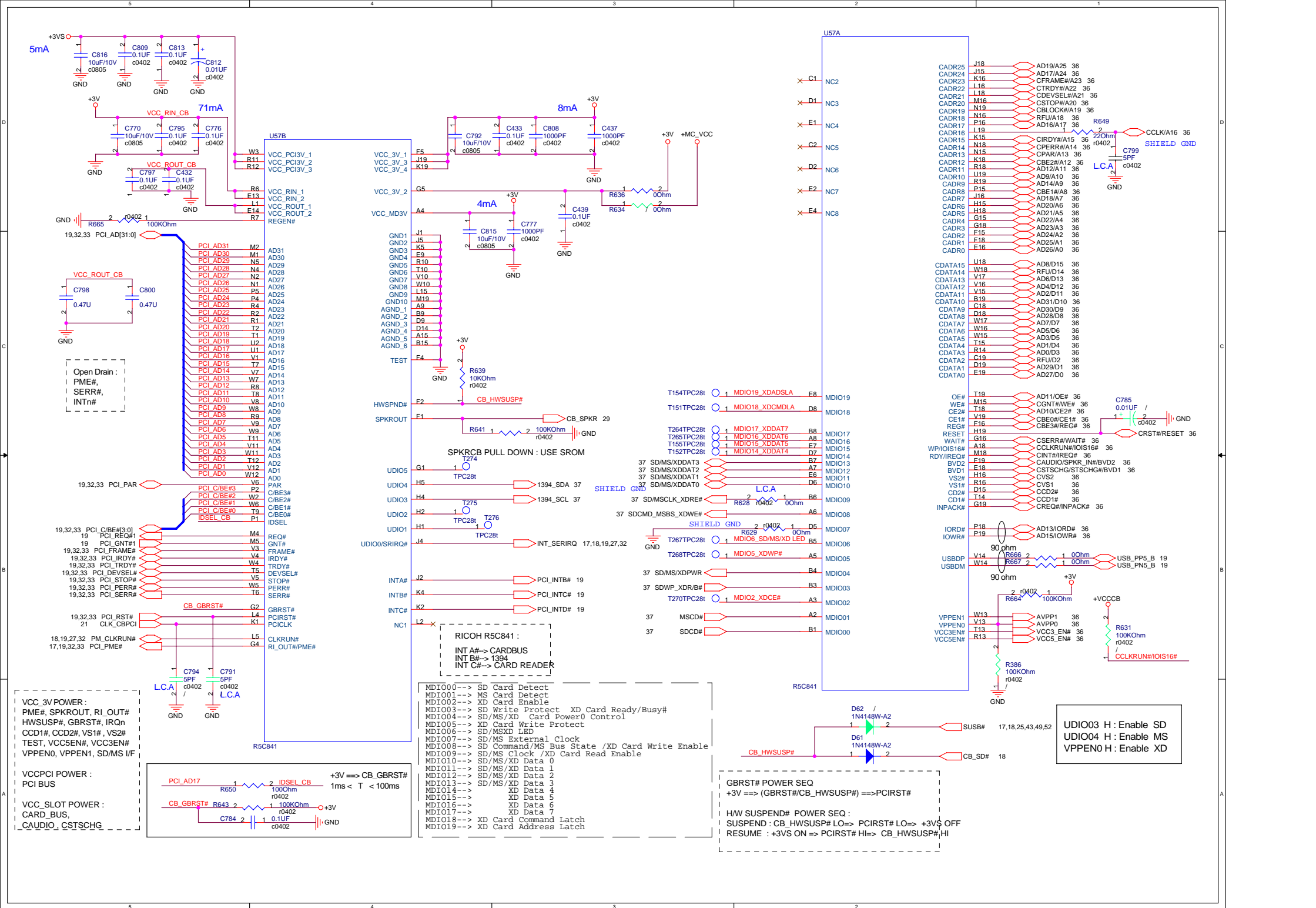
**LAN
PORT**

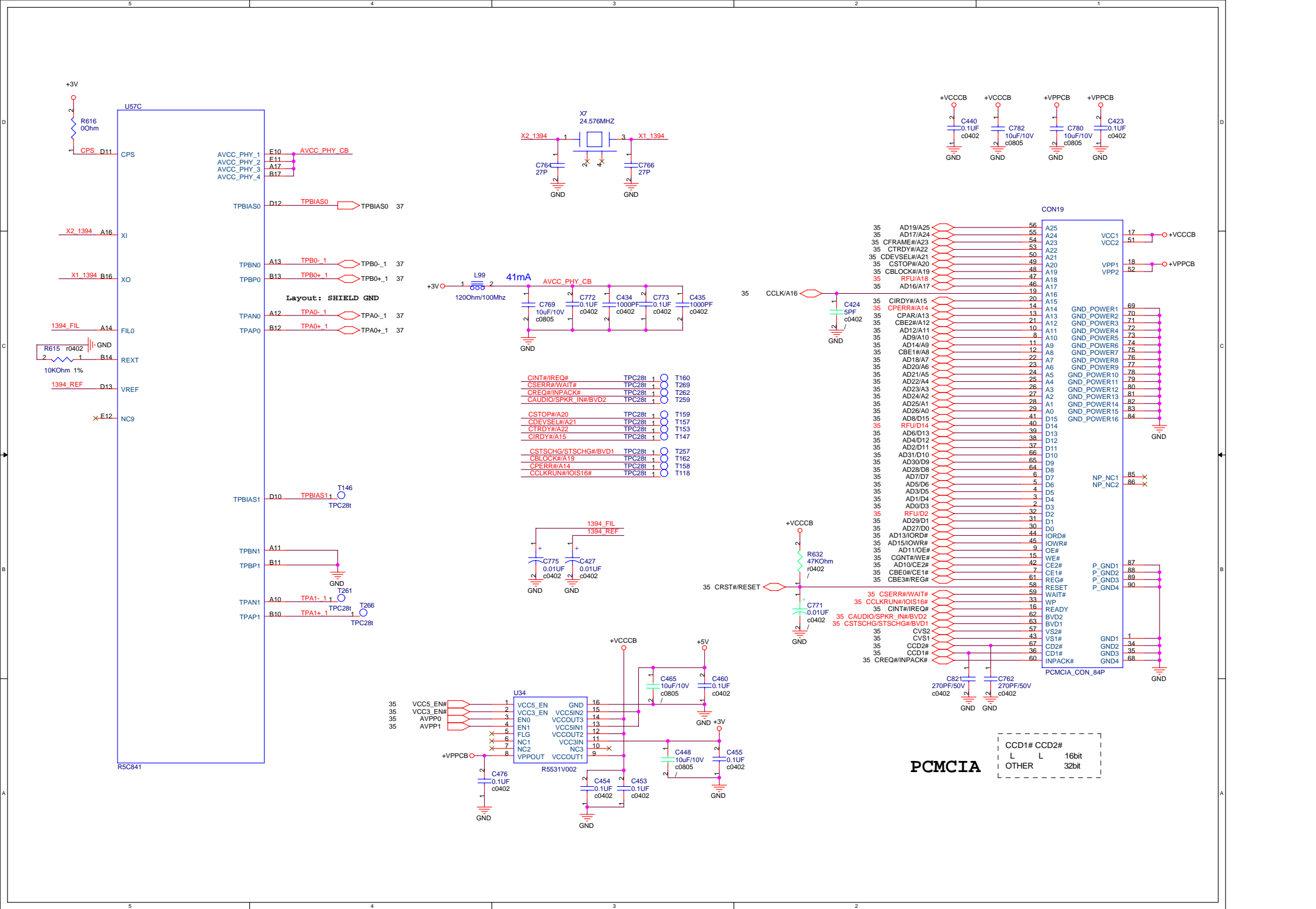


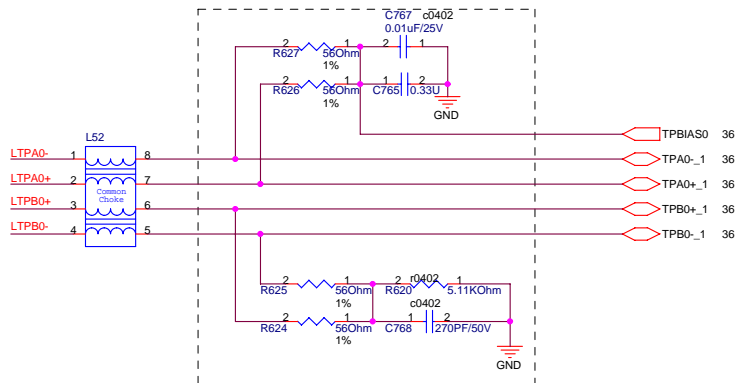
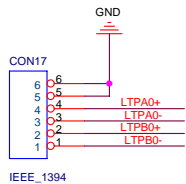
MDC



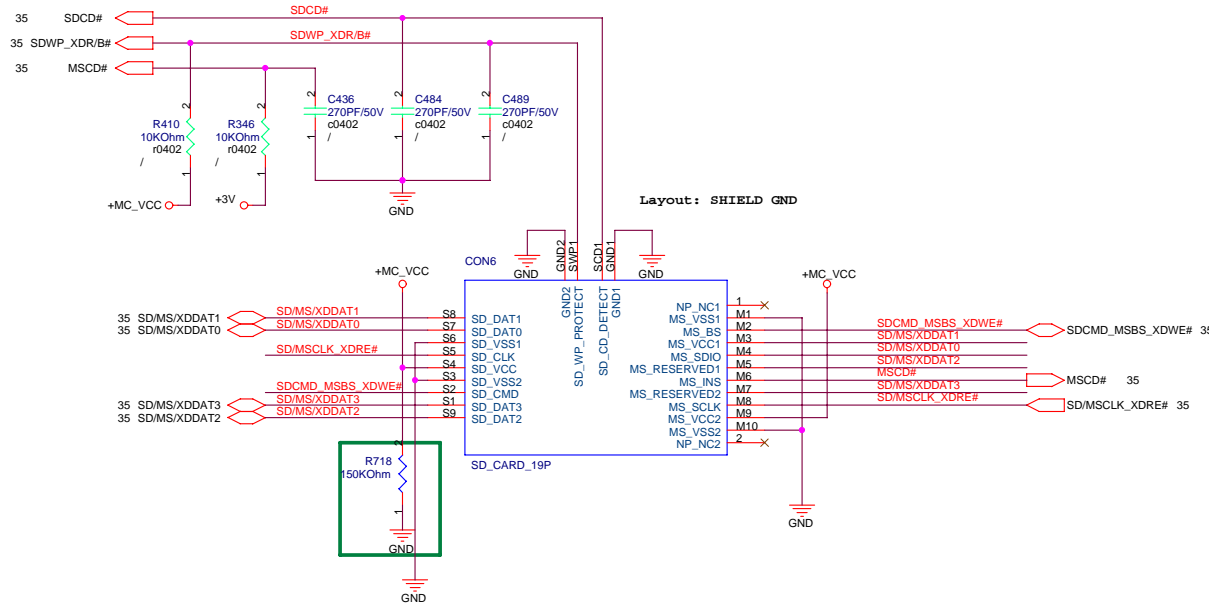
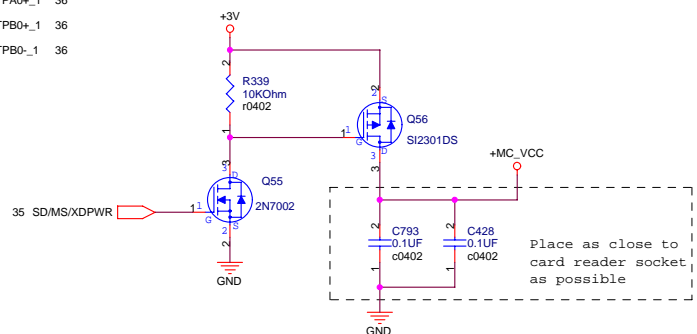
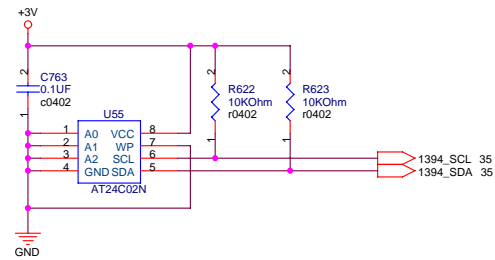
**Must change to
13-N7510M270**



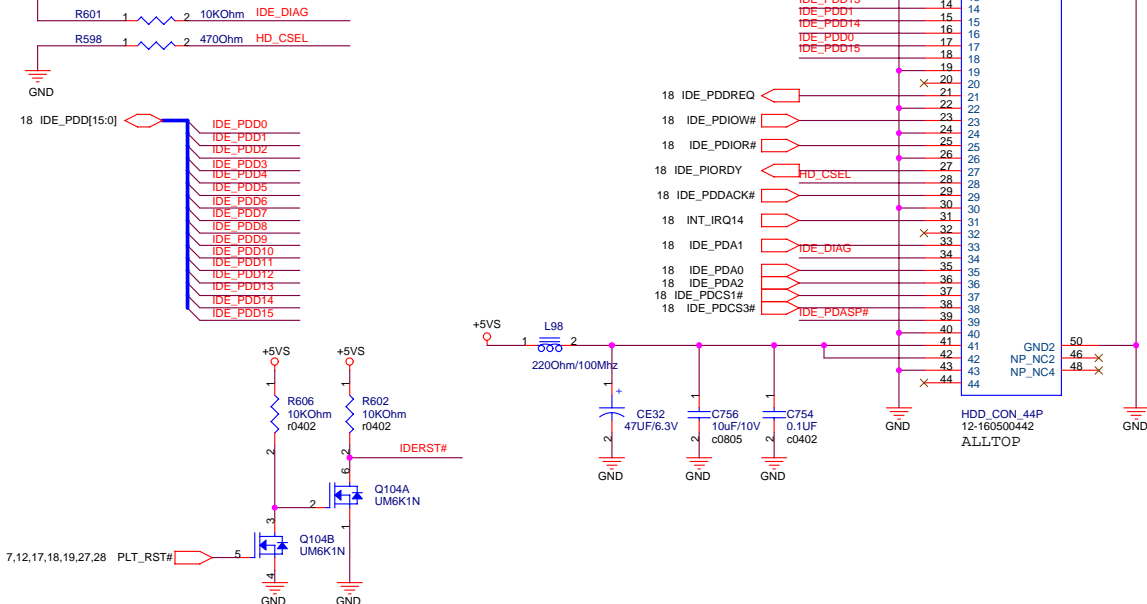




- 1.CLOSE TO R5C841
- 2.The area is as compact as possible,length < 10 mm
- 3.TPA Pair and TPB pair mismatch < 2.5mm
- 4.No via recommend , maximum is one.
- 5.Total length < 50 mm
- 6.Differential impedance is 110+/- 6 ohm
- 7.TPA Pair trace or TPB pair trace mismatch < 1.25mm

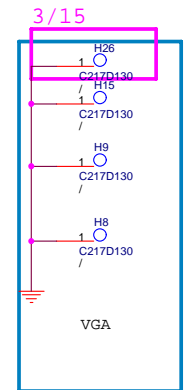
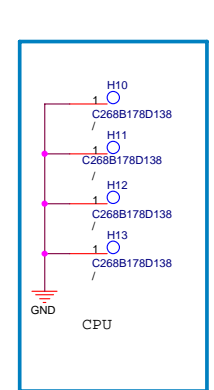
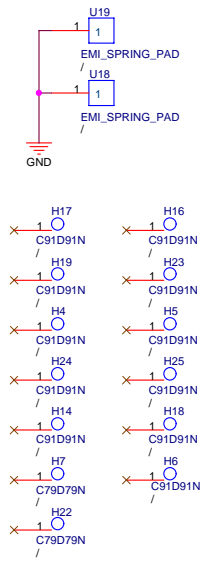
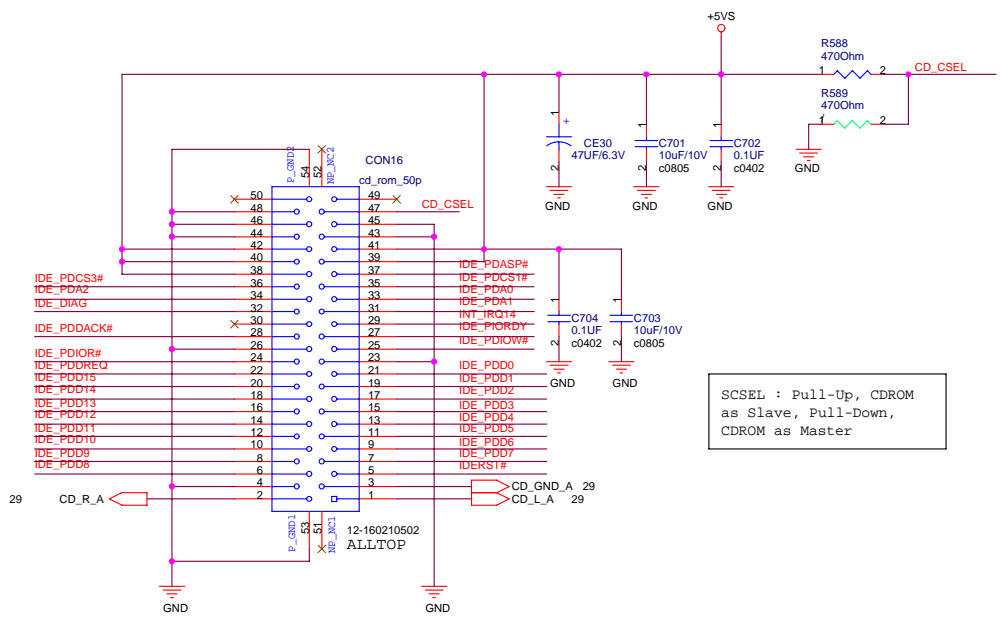


HD_CSEL : Pull-Down, HDD as Master



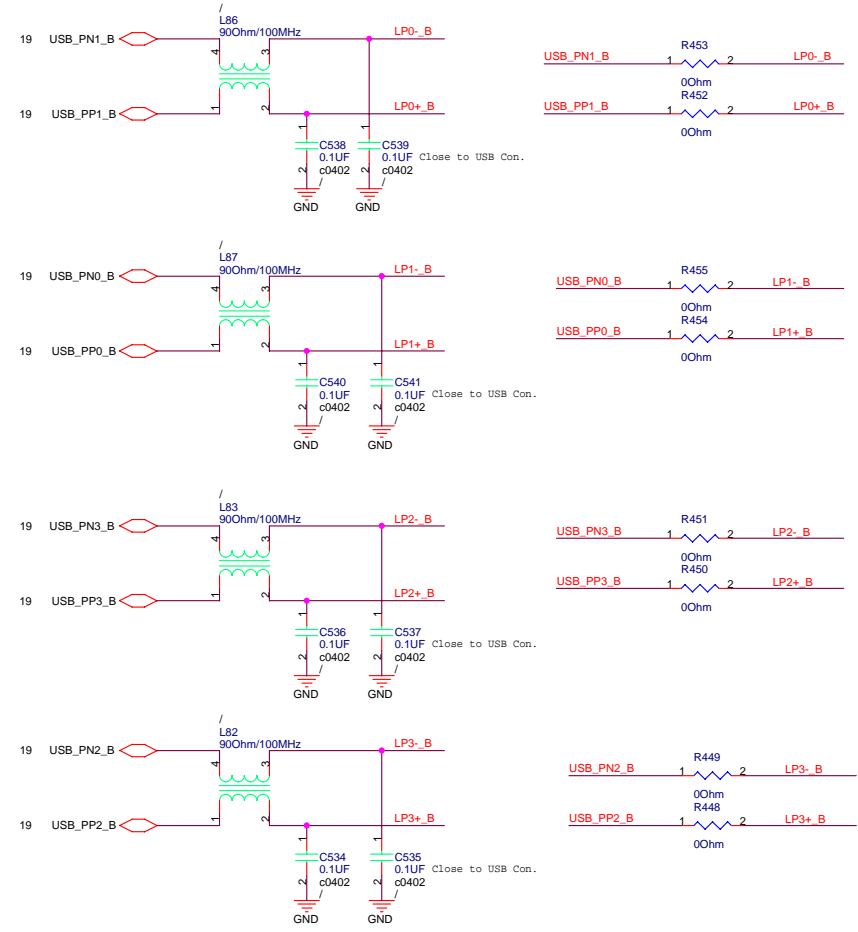
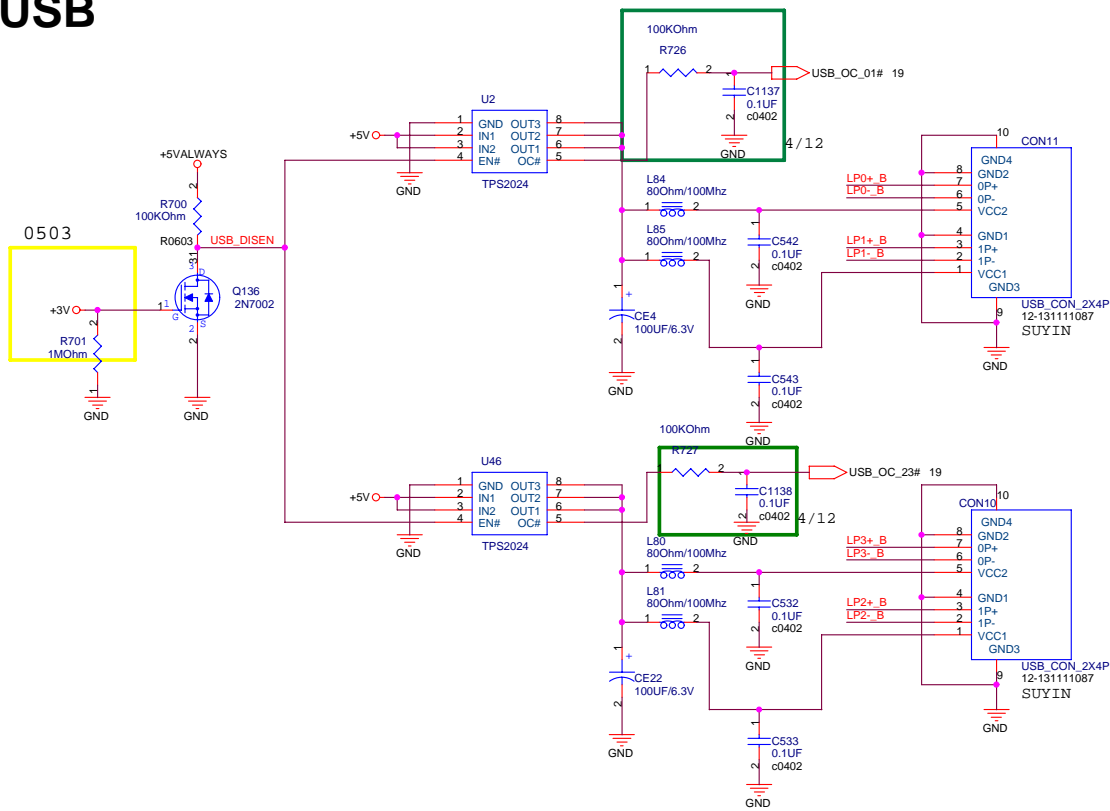
HDD

CD-ROM



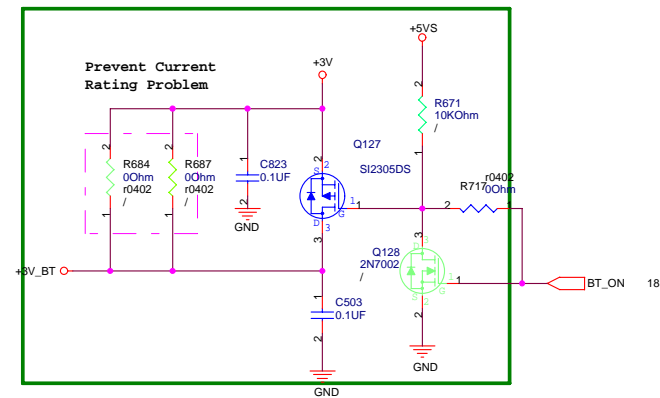
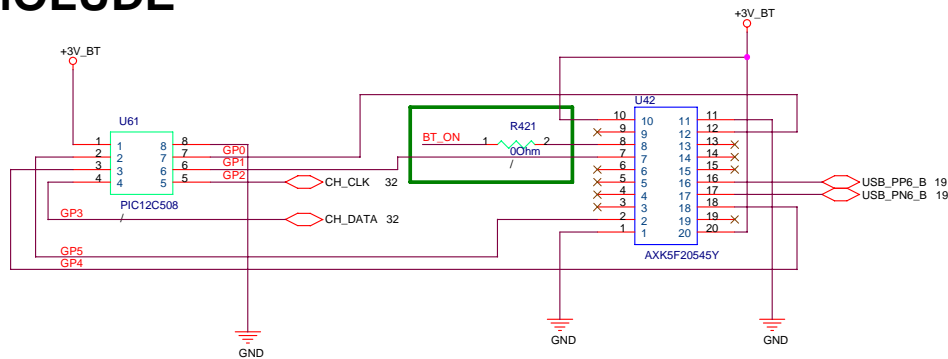
3/15

USB



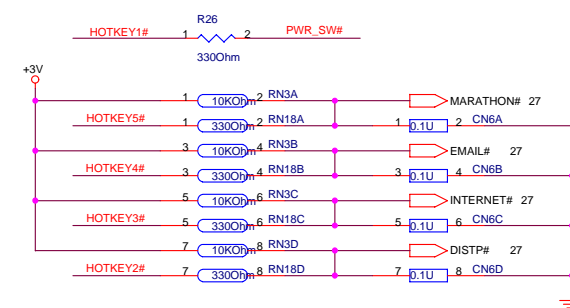
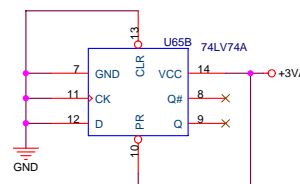
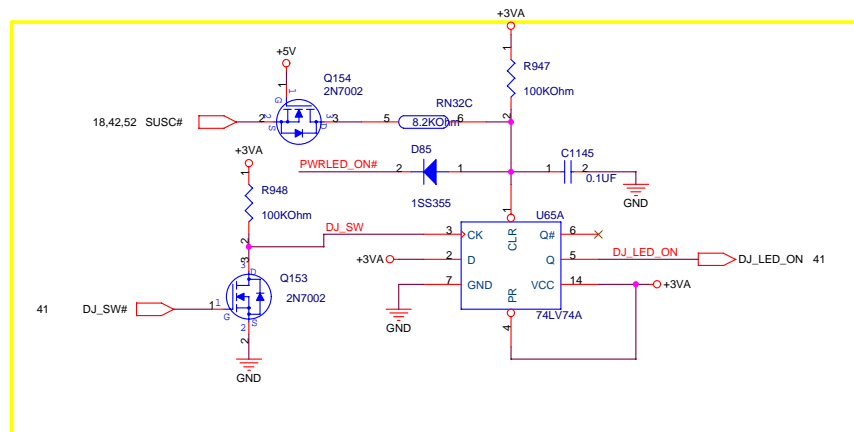
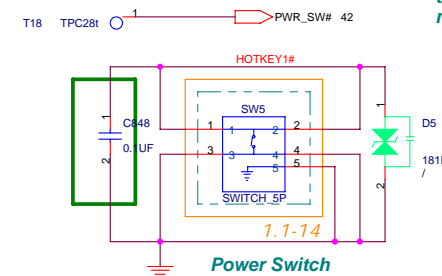
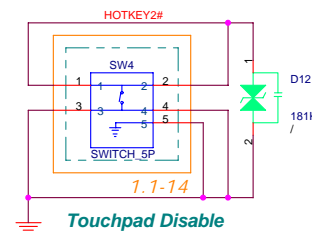
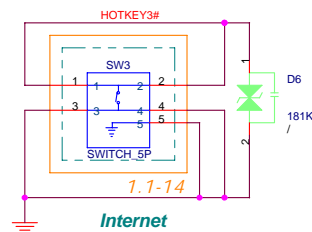
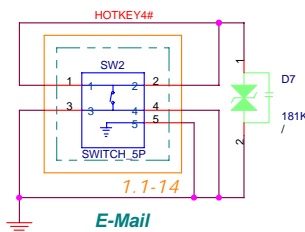
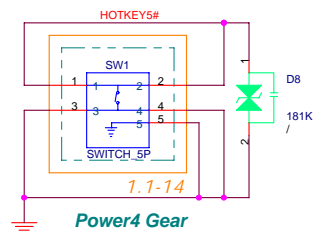
BLUE TOOTH

MOLUDE

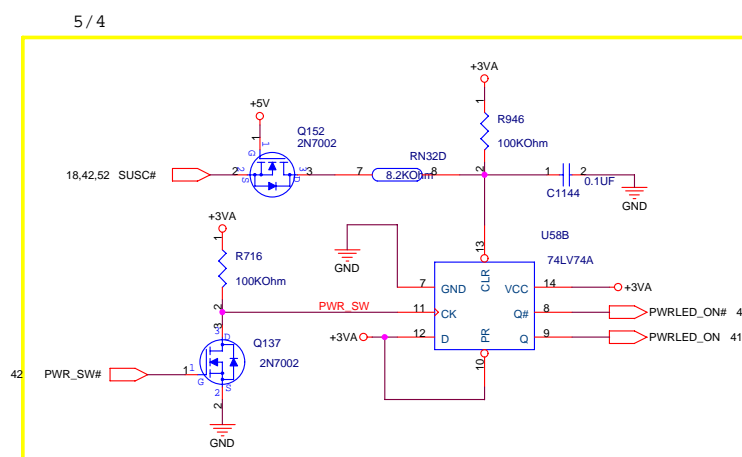
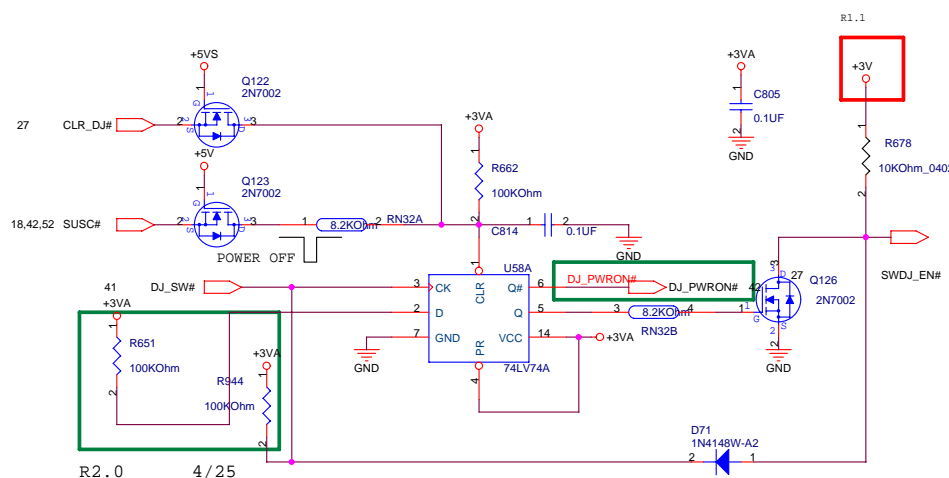


FUNCTION KEY

Uses 5-pin switch to improve ESD margin.



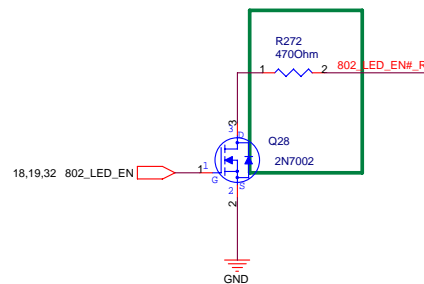
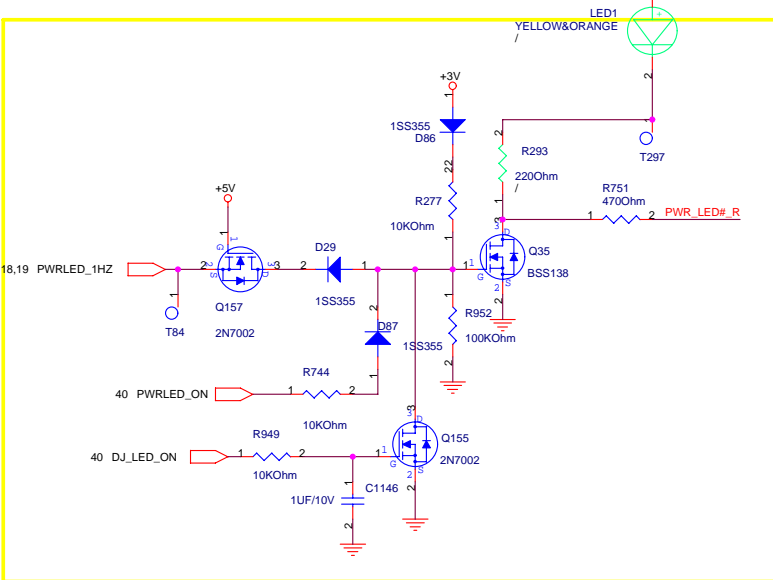
5 / 4



5 / 4

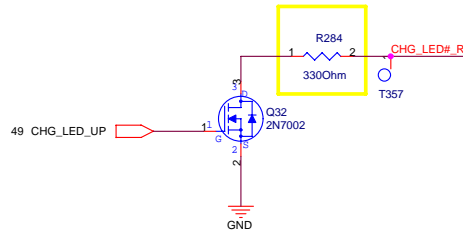
R2.0 4 / 25

POWER_LED

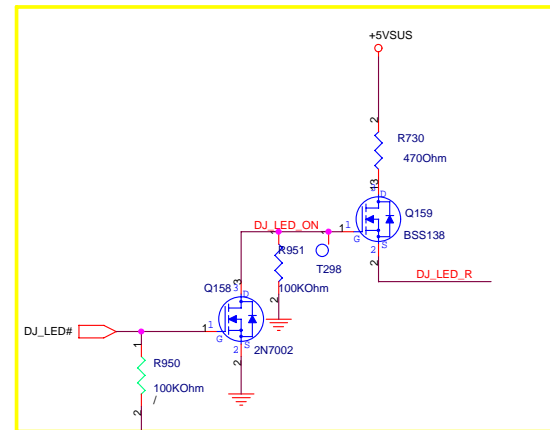


802_LED

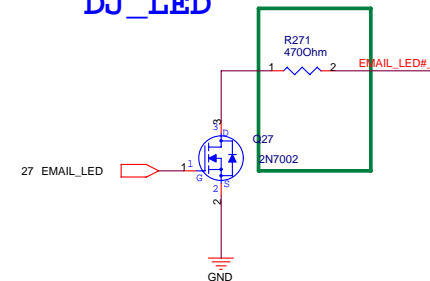
5/3 R2.0



CHG_LED



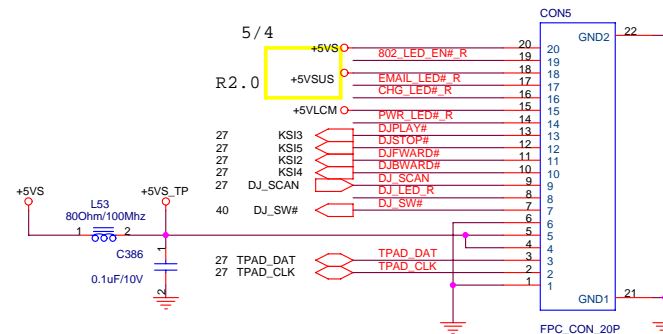
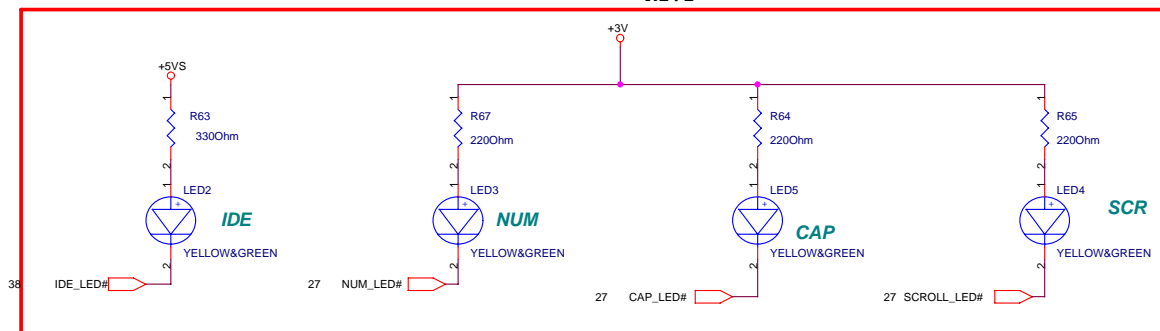
DJ_LED

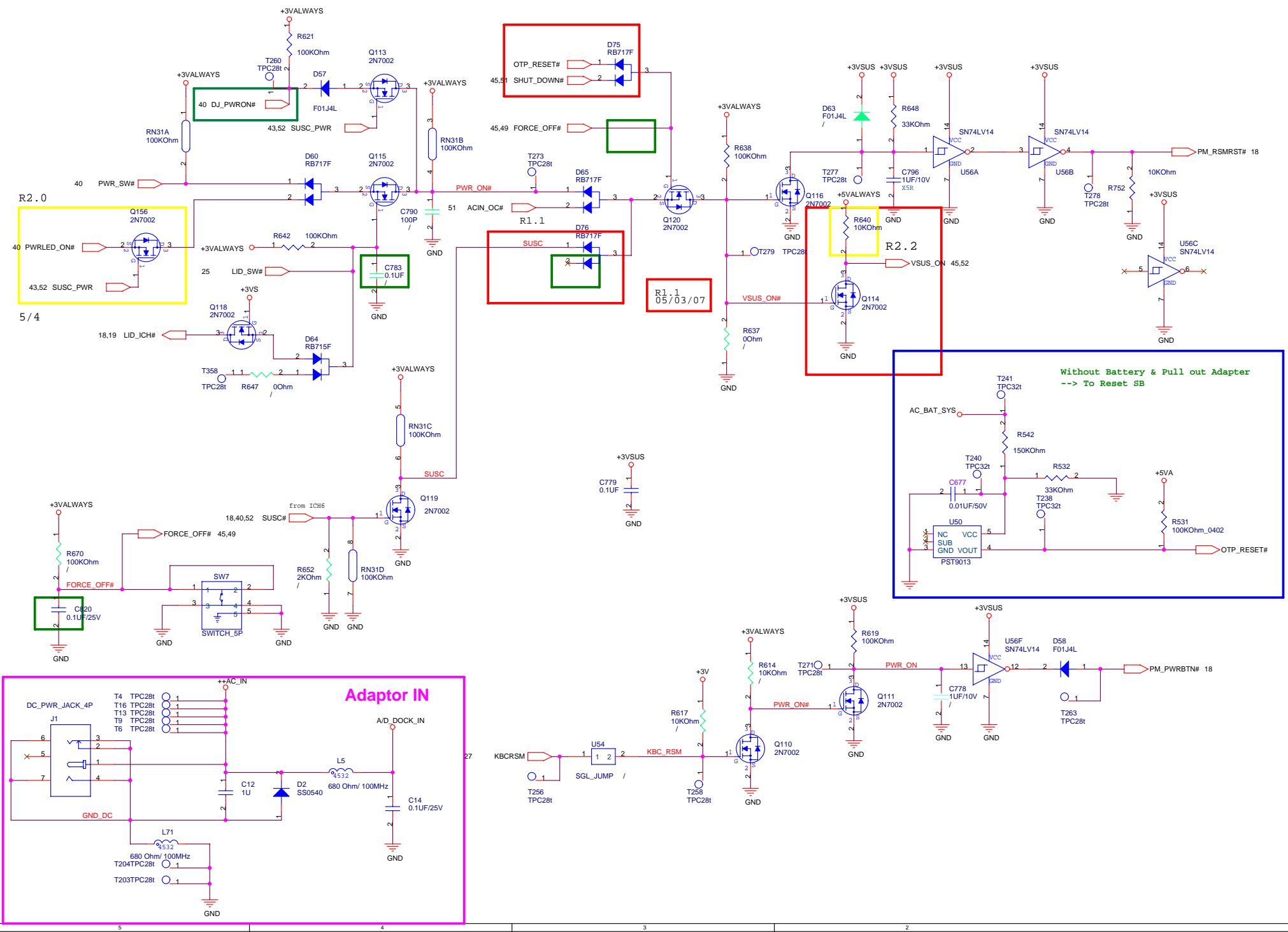


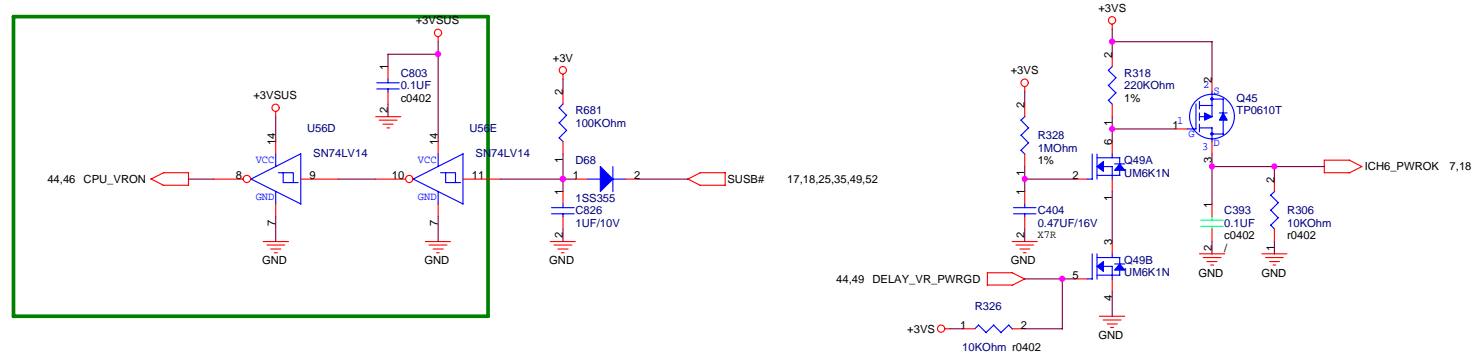
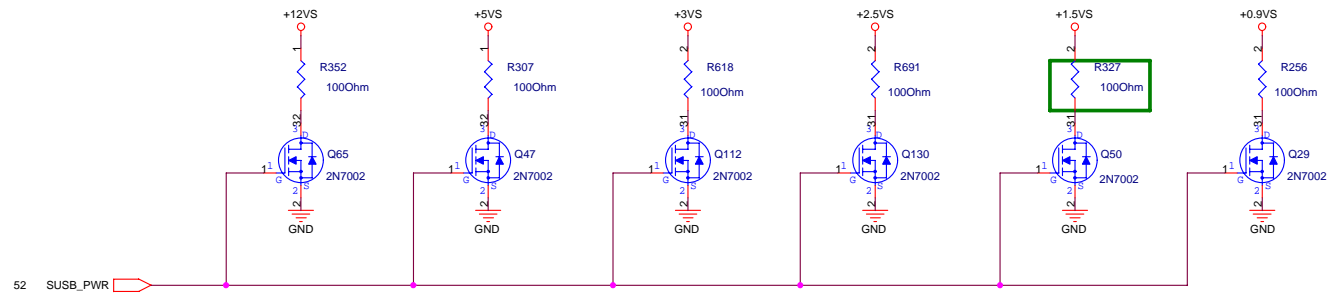
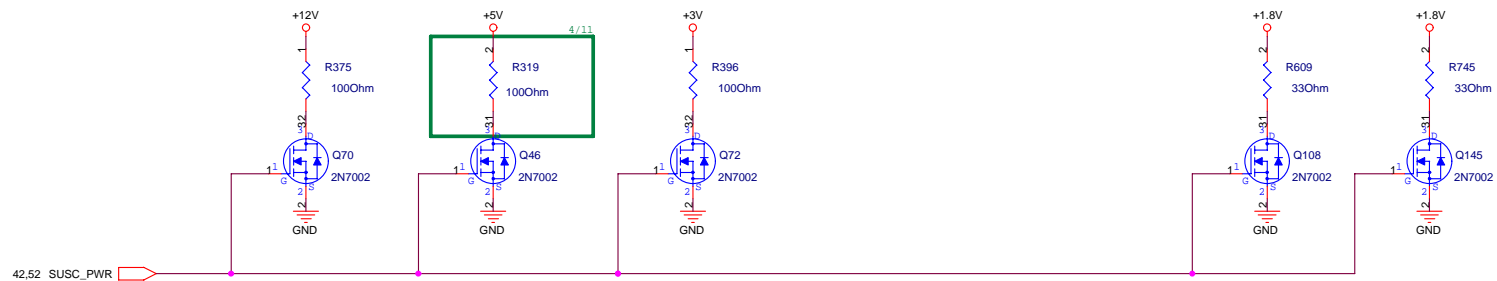
EMAIL_LED

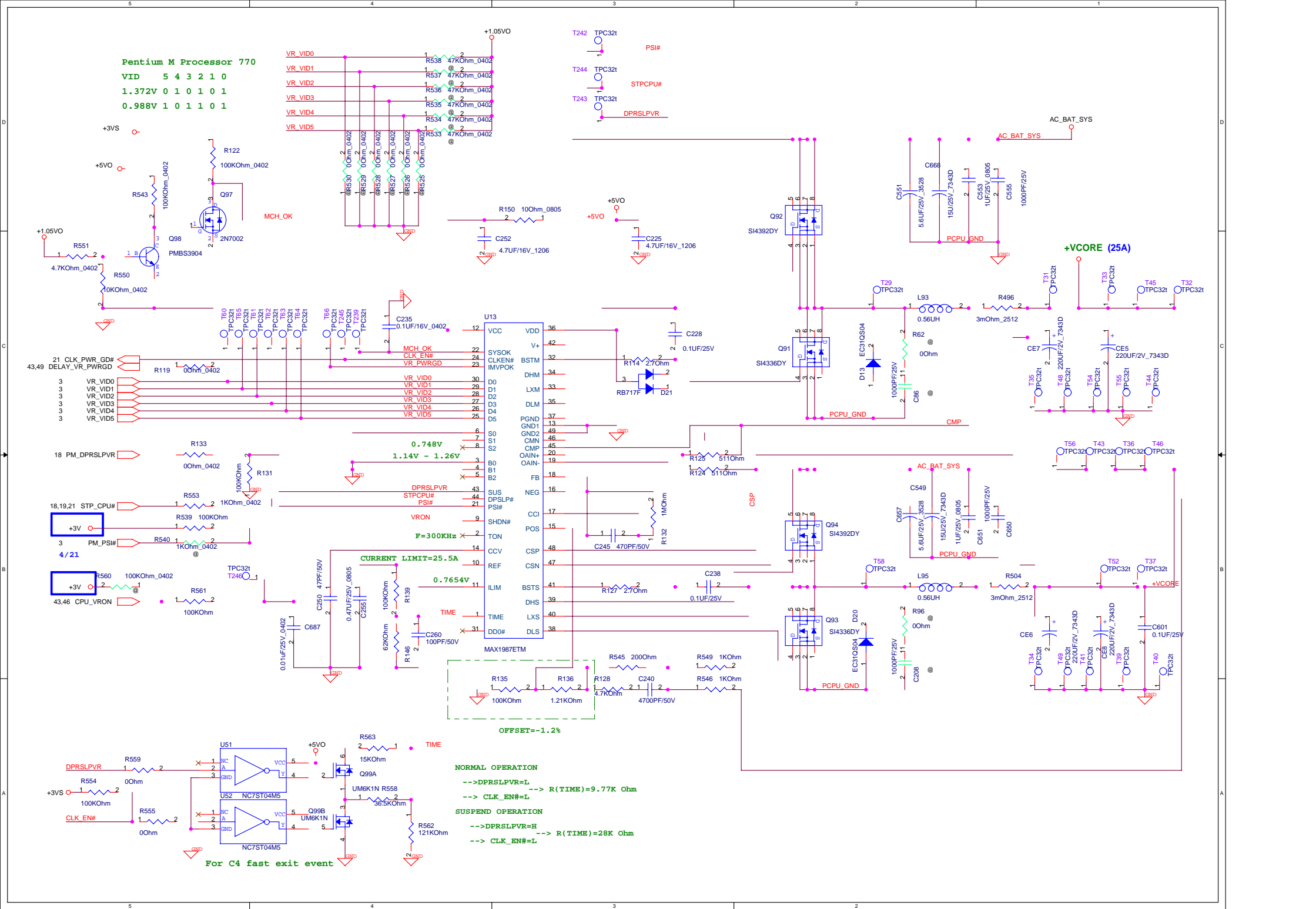
R2.0

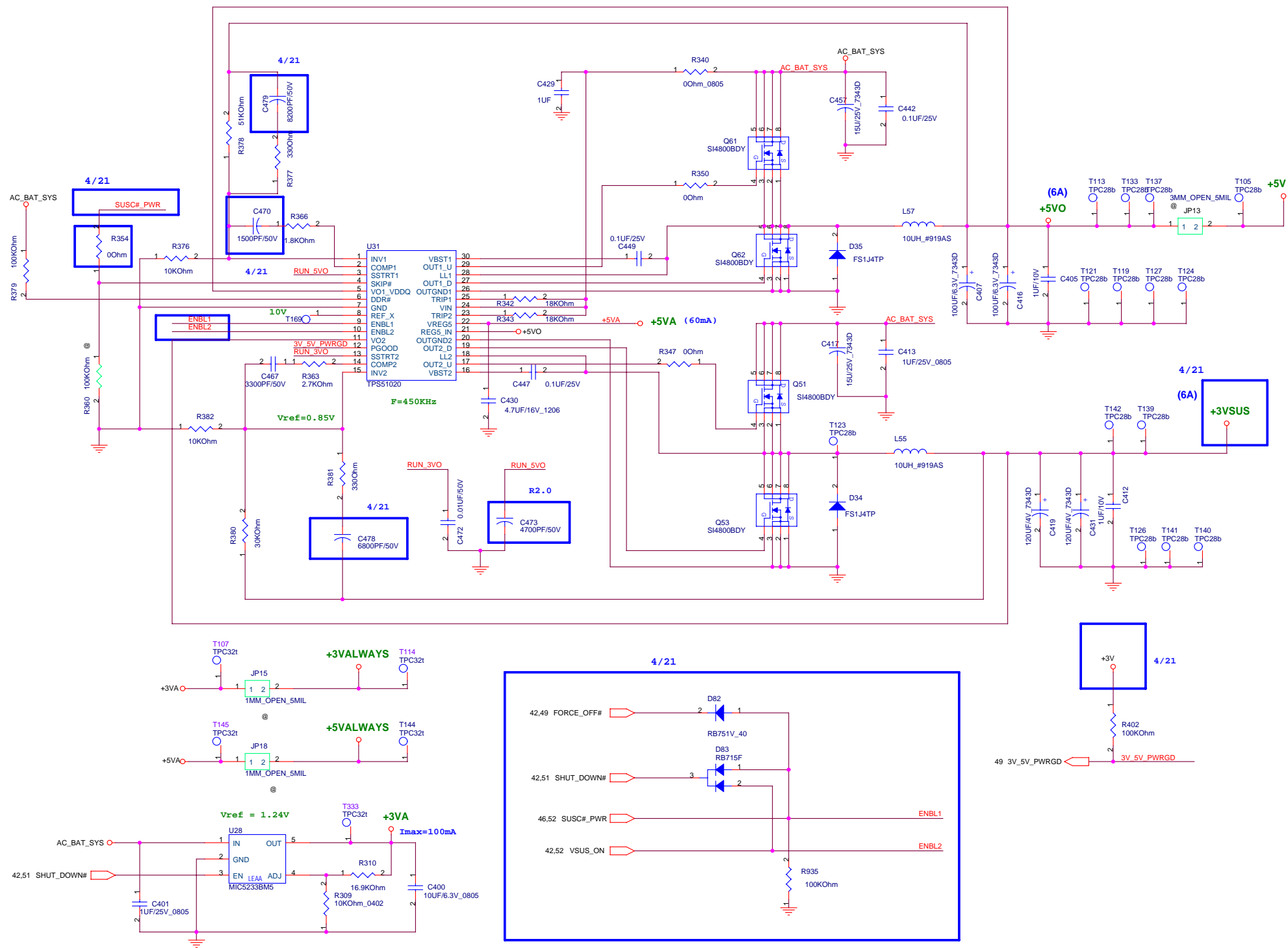
R1.1

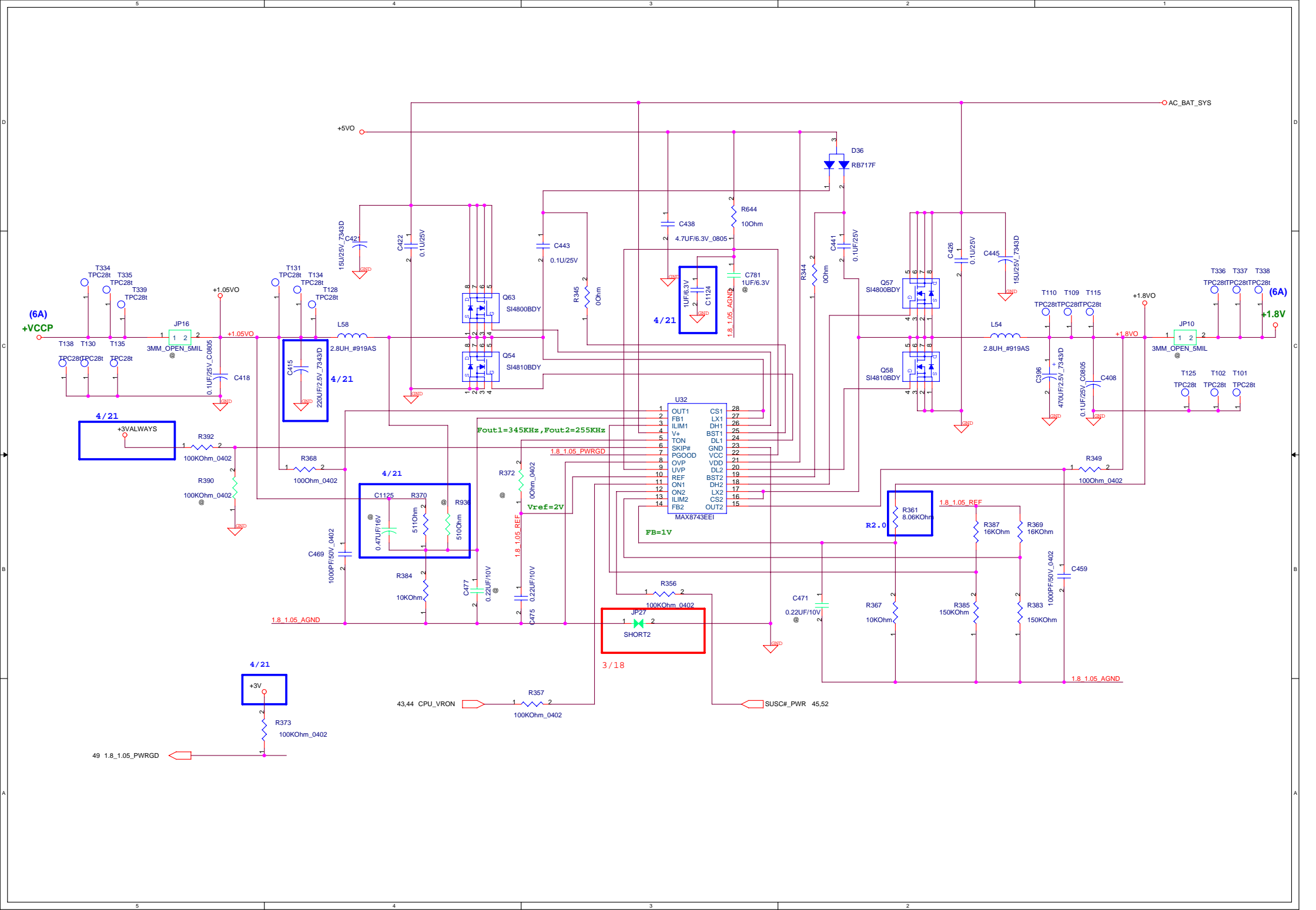


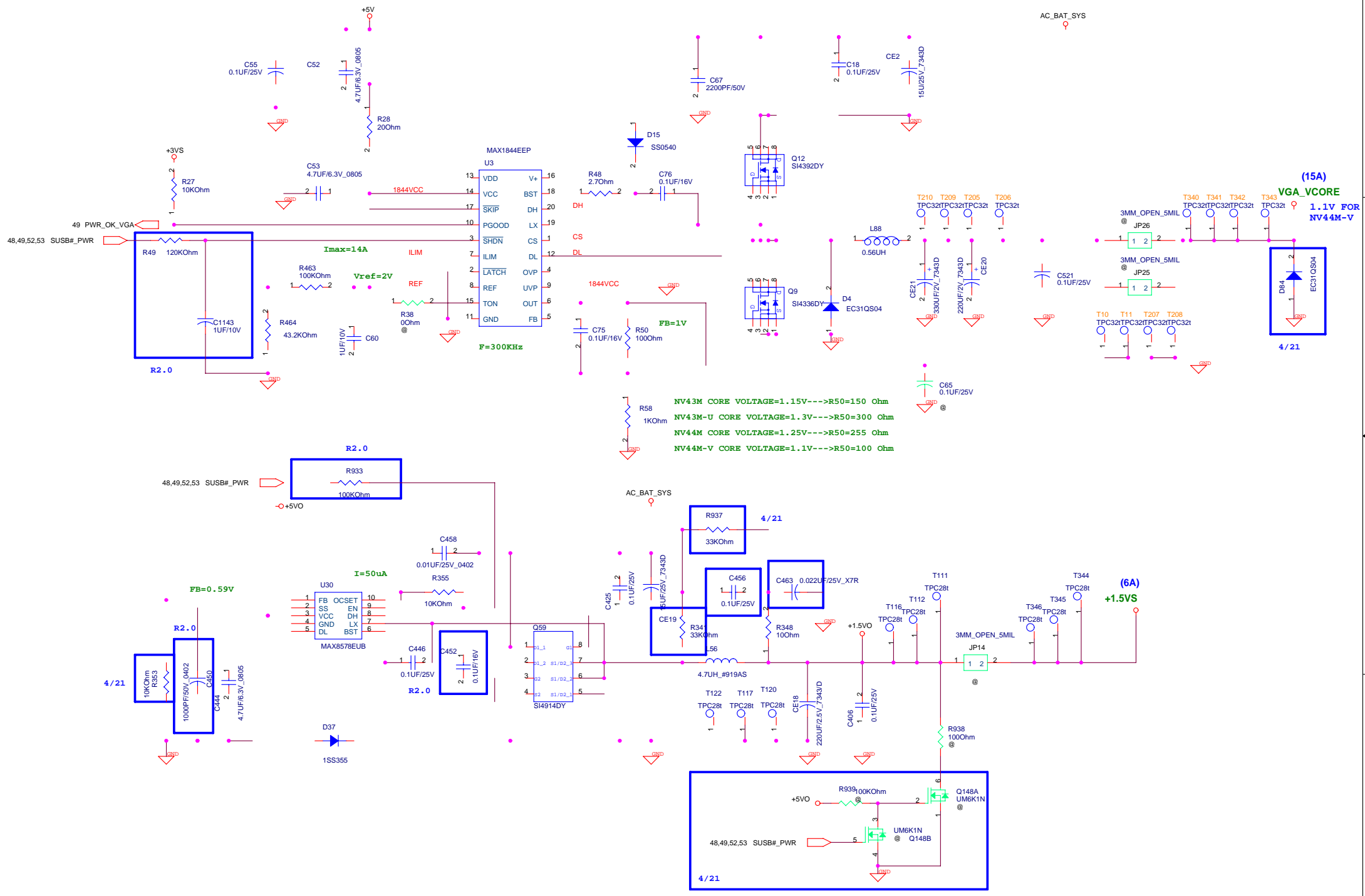




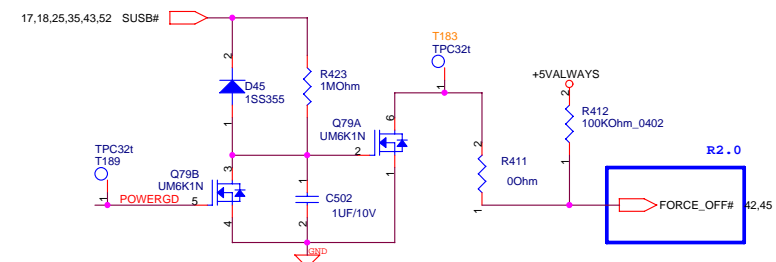
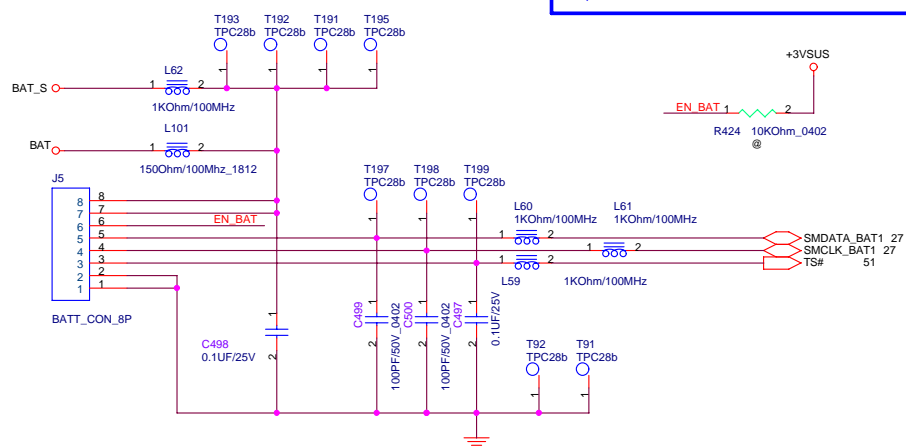
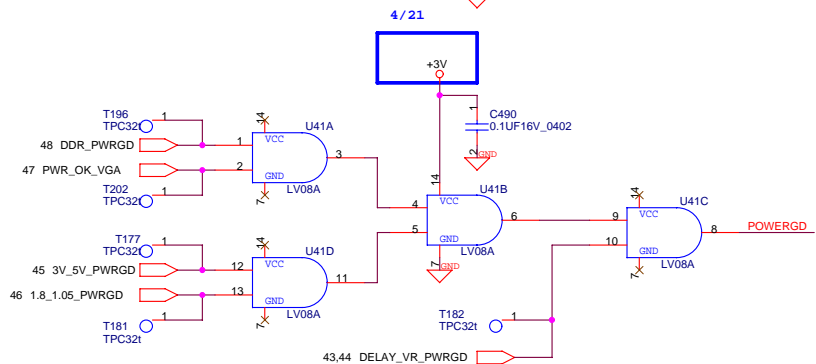
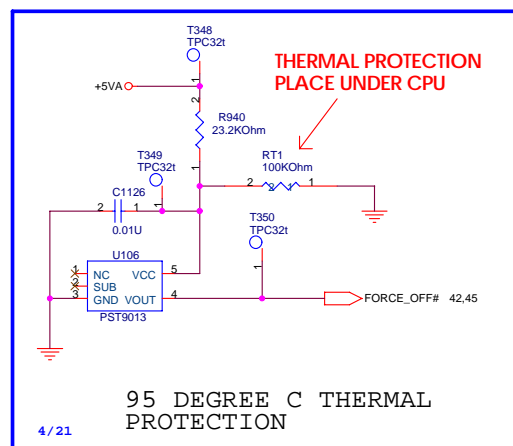
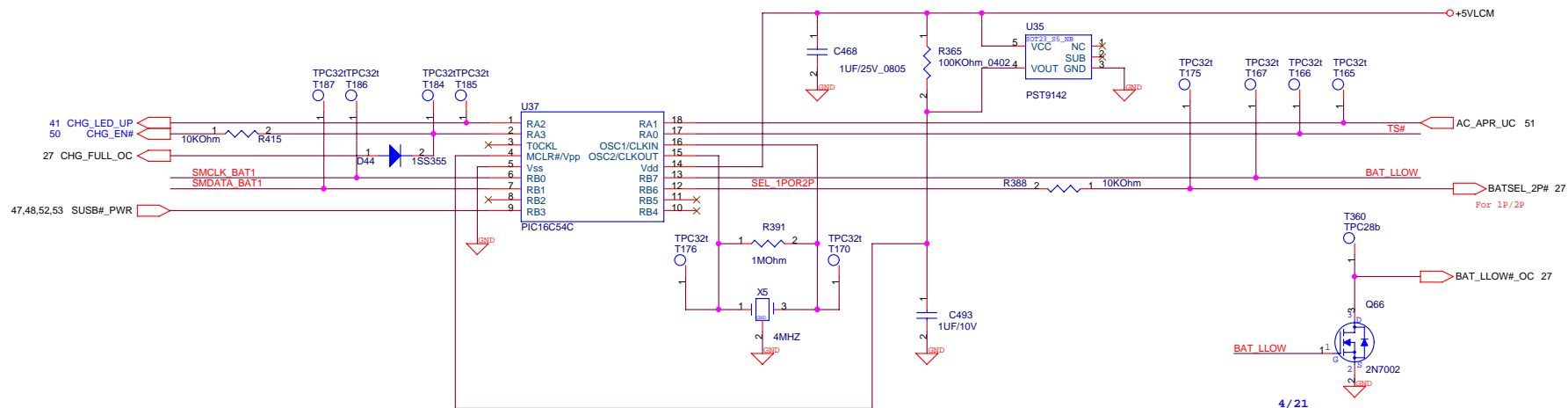


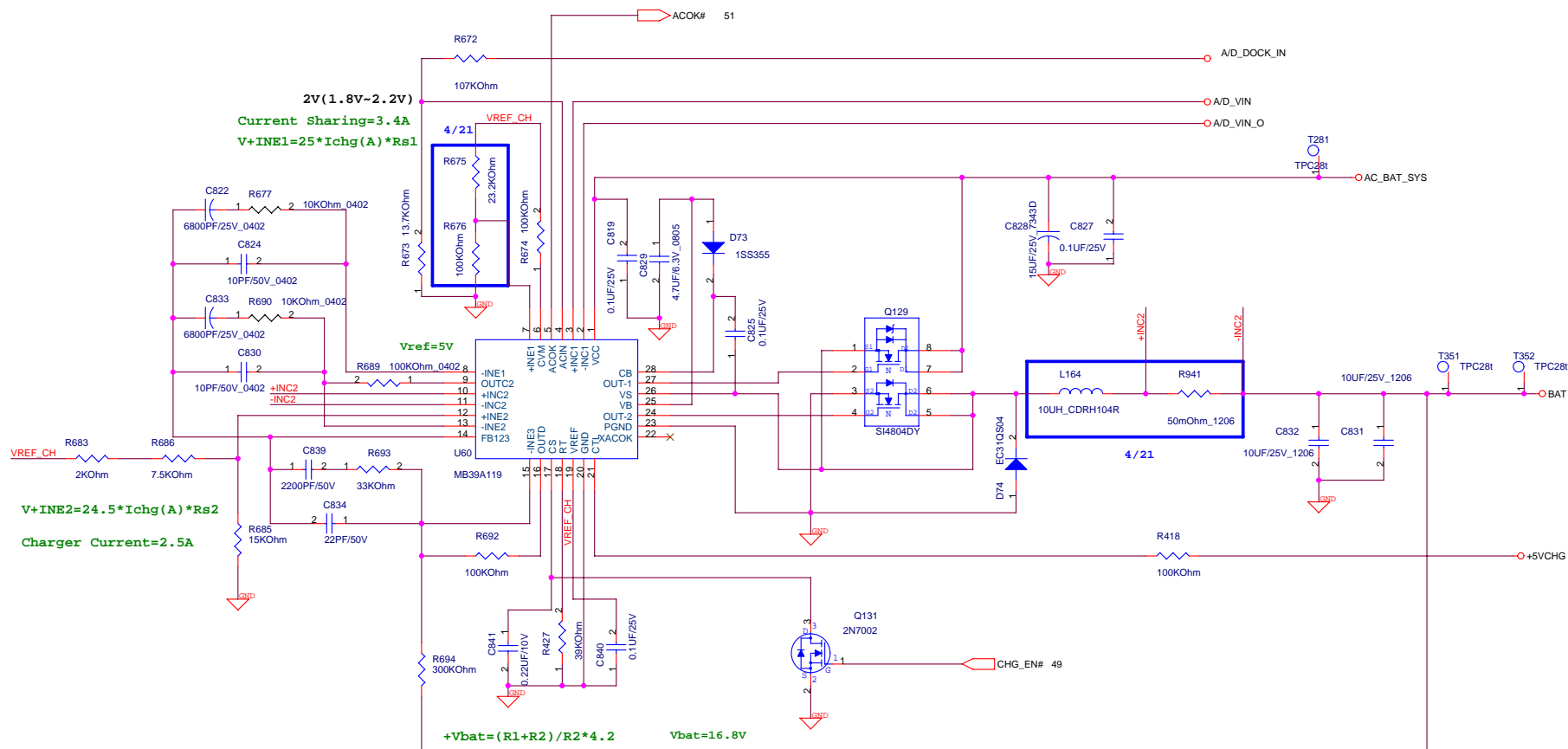


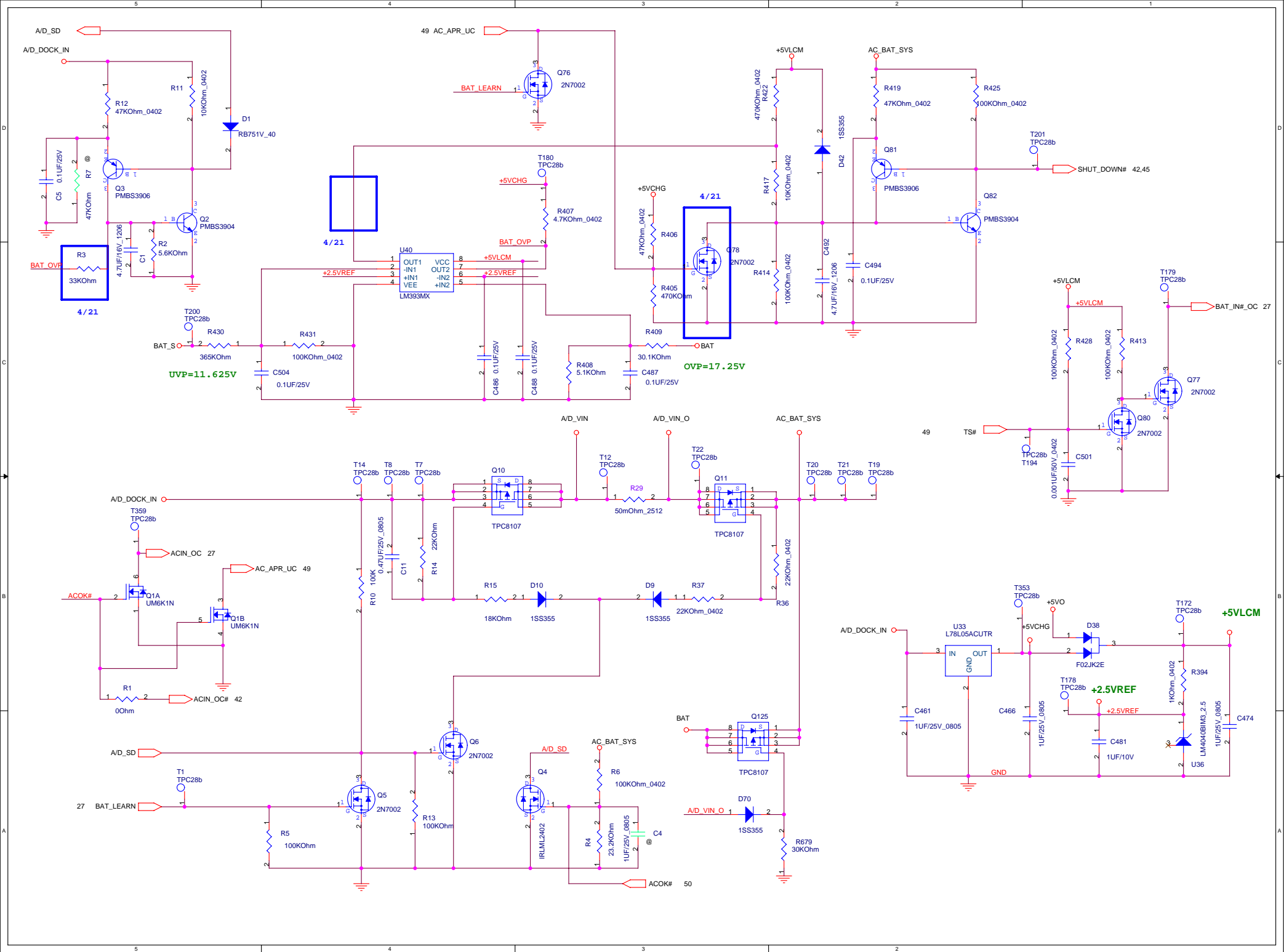


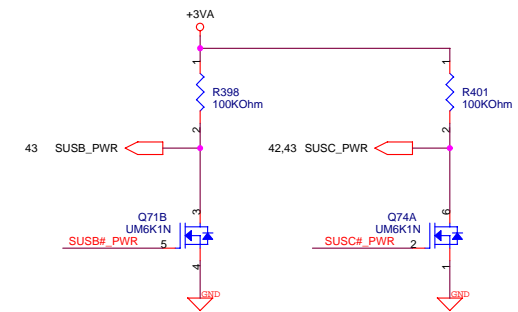
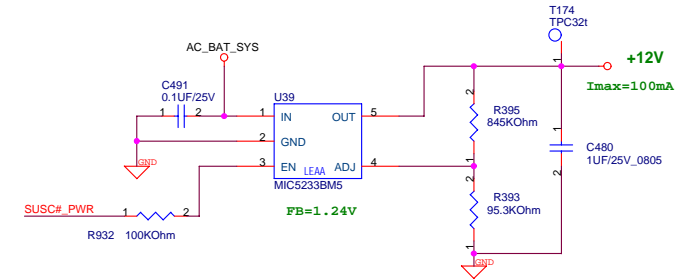
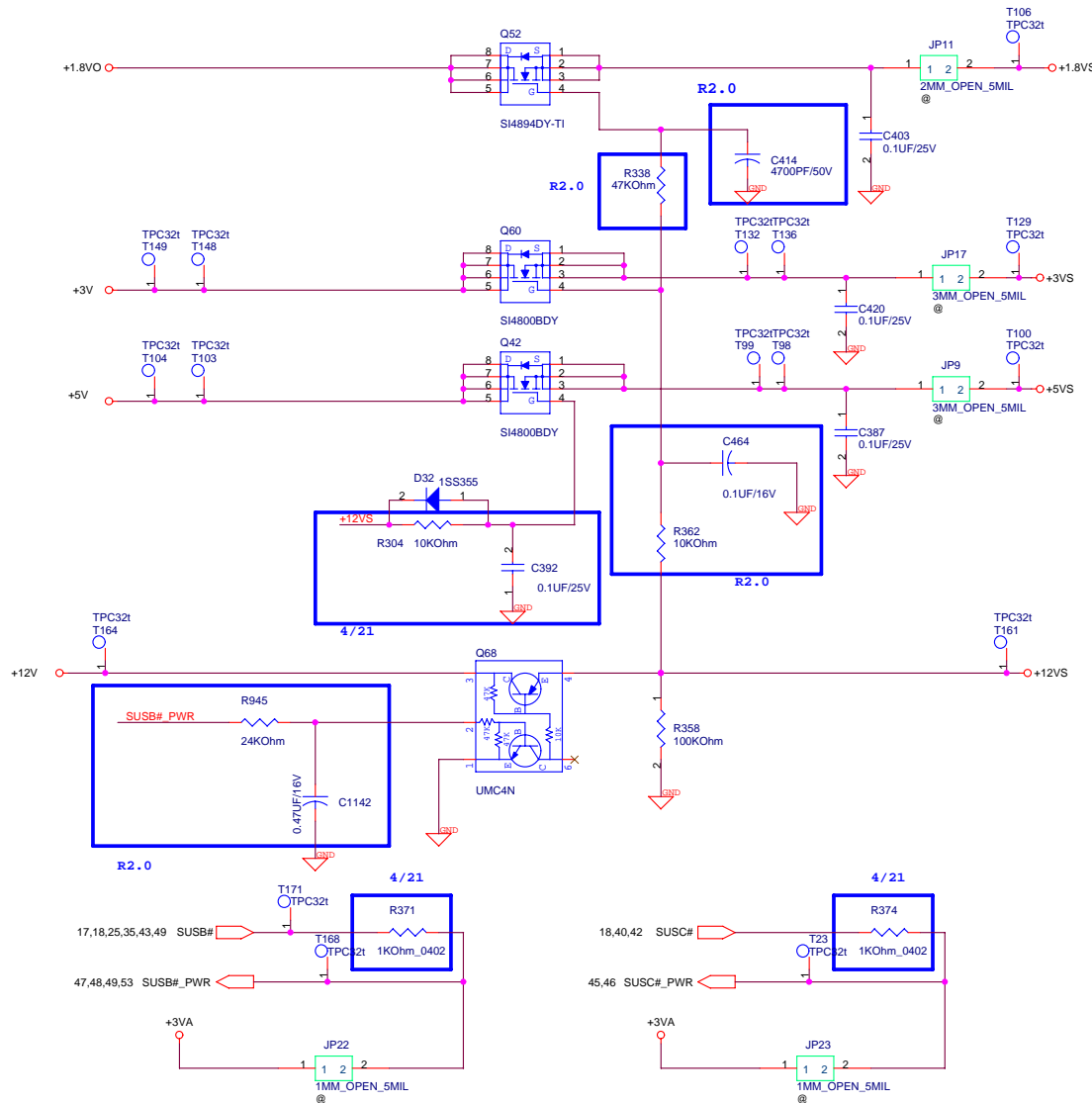
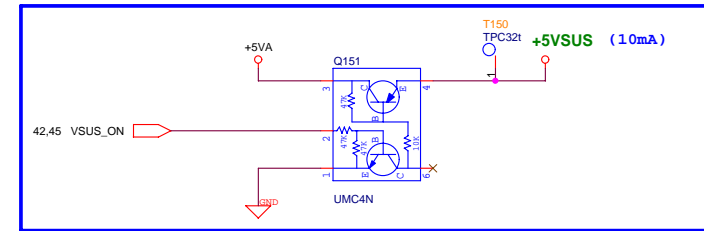
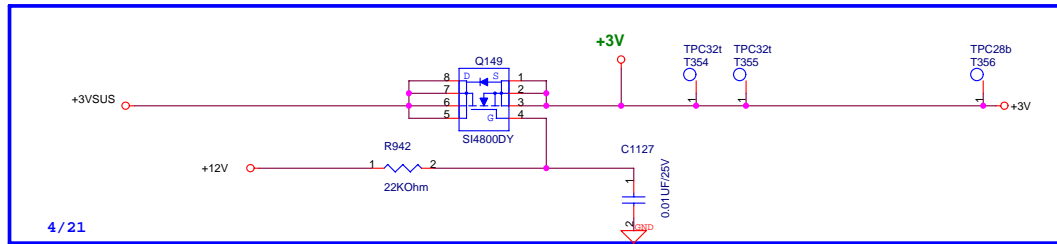


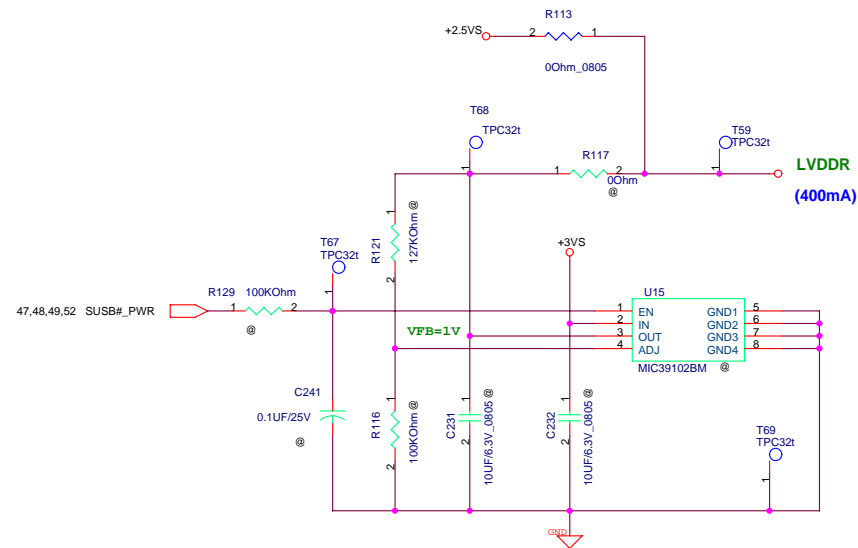
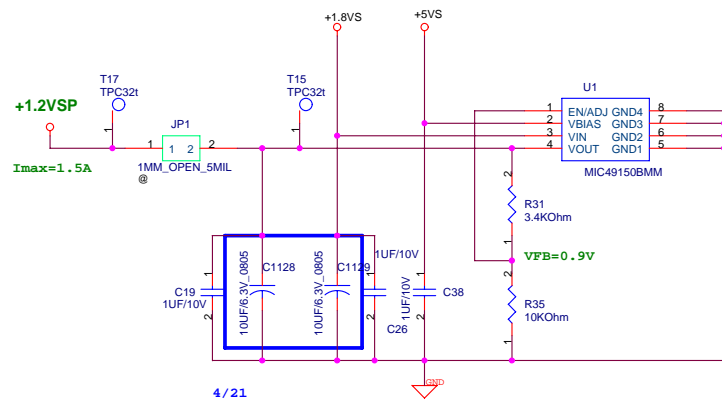




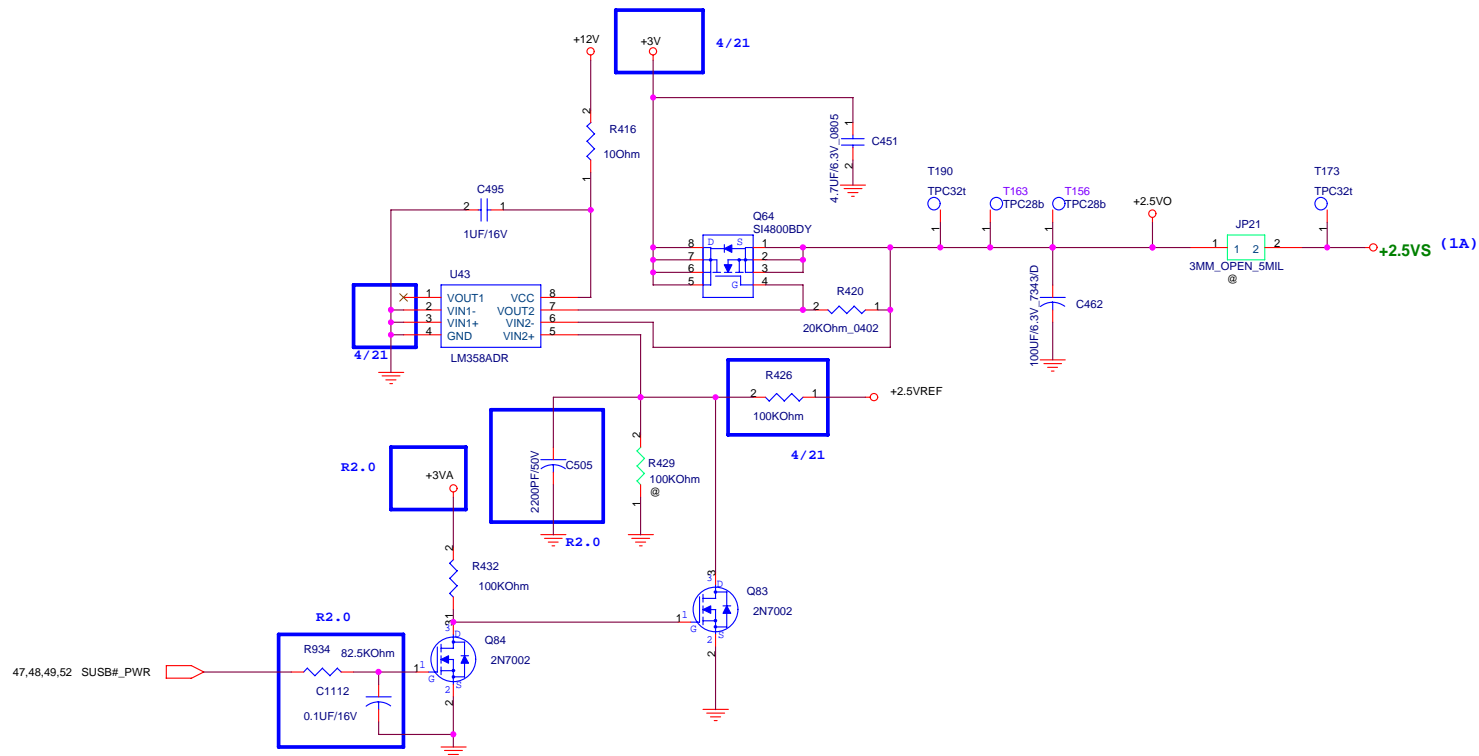


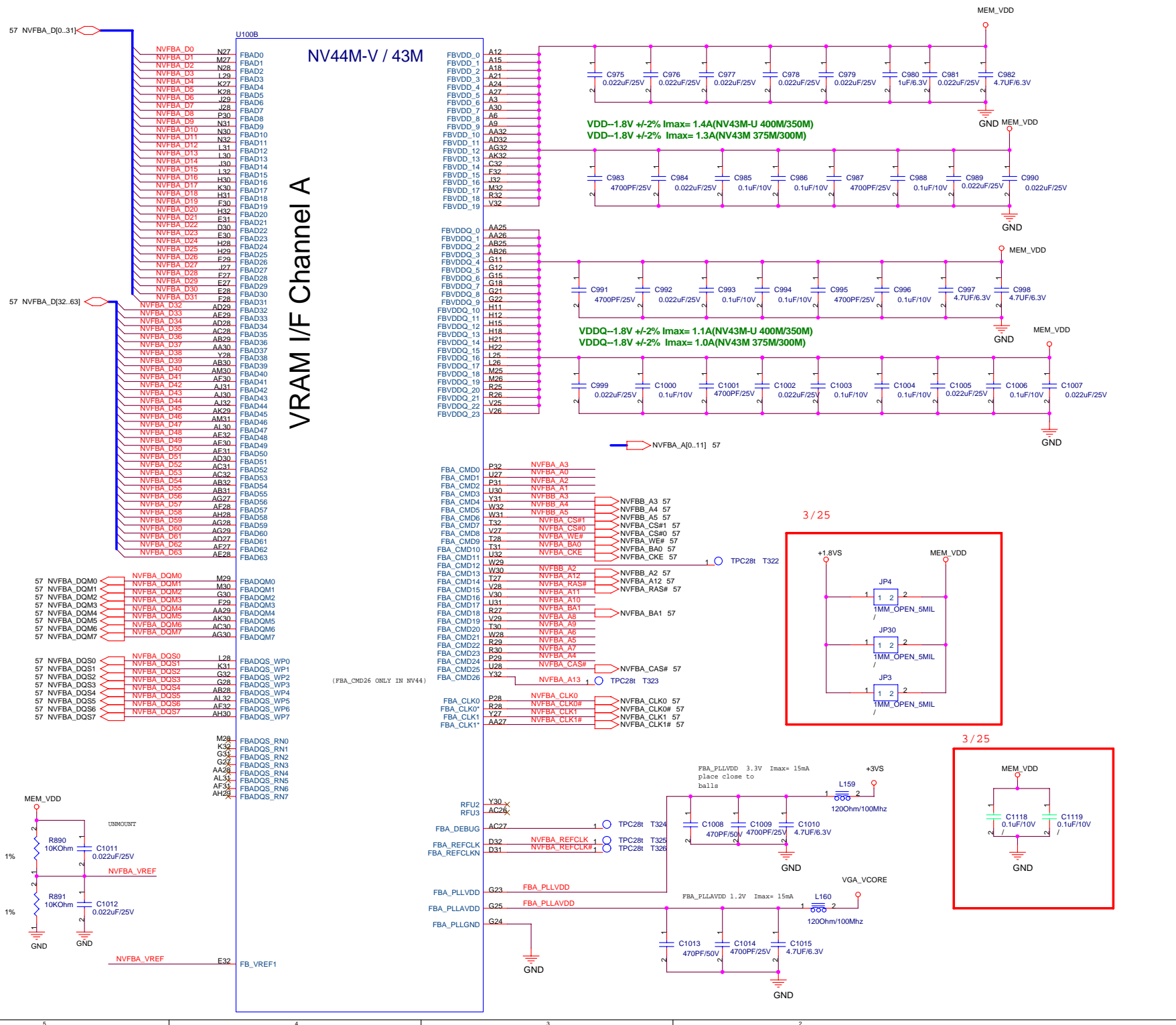






VGA PART





58 NVFBC_D[0..31]

58 NVFBC_D[32..63]

58 NVFBC_DQM0
58 NVFBC_DQM1
58 NVFBC_DQM2
58 NVFBC_DQM3
58 NVFBC_DQM4
58 NVFBC_DQM5
58 NVFBC_DQM6
58 NVFBC_DQM7

58 NVFBC_DQS0
58 NVFBC_DQS1
58 NVFBC_DQS2
58 NVFBC_DQS3
58 NVFBC_DQS4
58 NVFBC_DQS5
58 NVFBC_DQS6
58 NVFBC_DQS7

NVFBC_D0
NVFBC_D1
NVFBC_D2
NVFBC_D3
NVFBC_D4
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NVFBC_DQS1
NVFBC_DQS2
NVFBC_DQS3
NVFBC_DQS4
NVFBC_DQS5
NVFBC_DQS6
NVFBC_DQS7

FBCDQ0_RN0
FBCDQ0_RN1
FBCDQ0_RN2
FBCDQ0_RN3
FBCDQ0_RN4
FBCDQ0_RN5
FBCDQ0_RN6
FBCDQ0_RN7

U100C

NV44M-V / 43M

VRAM I/F CHANNEL C
(ONLY FOR NV43)

FB_VREF2

FBVTT_0
FBVTT_1
FBVTT_2
FBVTT_3
FBVTT_4
FBVTT_5
FBVTT_6
FBVTT_7
FBVTT_8
FBVTT_9
FBVTT_10
FBVTT_11
FBVTT_12
FBVTT_13
FBVTT_14
FBVTT_15
FBVTT_16
FBVTT_17

FBC_CMD0
FBC_CMD1
FBC_CMD2
FBC_CMD3
FBC_CMD4
FBC_CMD5
FBC_CMD6
FBC_CMD7
FBC_CMD8
FBC_CMD9
FBC_CMD10
FBC_CMD11
FBC_CMD12
FBC_CMD13
FBC_CMD14
FBC_CMD15
FBC_CMD16
FBC_CMD17
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FBC_CMD24
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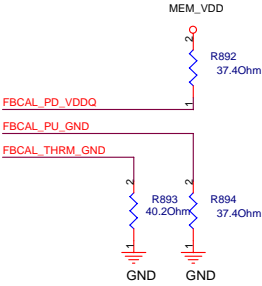
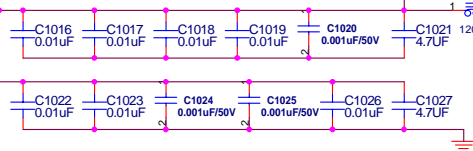
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FBC_CLK1
FBC_CLK1#

RFU4
RFU5
FBC_DEBUG
FBC_REFCLK
FBC_REFCLKN

FBC_PLLVDD
FBC_PLLAVDD
FBC_PL LGND

FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND

AA23
AB23
H16
H17
J10
J23
J24
J9
K11
K12
K21
K22
K24
K9
L23
M23
T25
U25



NVFBC_A[0..11] 58

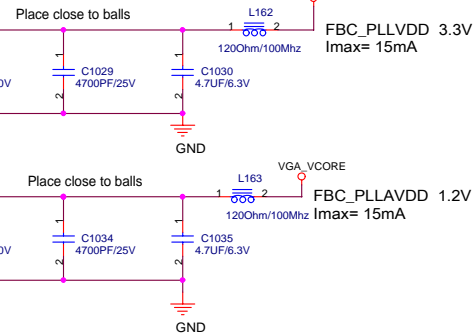
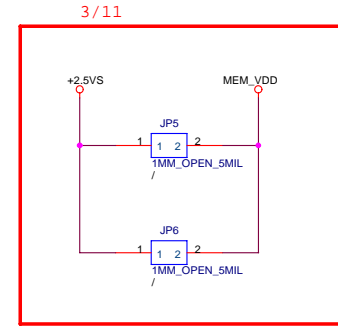
NVFBC_A3
NVFBC_A0
NVFBC_A2
NVFBC_A1
NVFBD_A3 58
NVFBD_A4 58
NVFBD_A5 58
NVFBC_CS#1
NVFBC_CS#0 58
NVFBC_WE#
NVFBC_WE# 58
NVFBC_BA0
NVFBC_BA0 58
NVFBC_CKE
NVFBC_CKE 58
NVFBD_A2
NVFBD_A2 58
NVFBC_RAS#
NVFBC_RAS# 58
NVFBC_A10
NVFBC_BA1 58
NVFBC_A8
NVFBC_A9
NVFBC_A5
NVFBC_A7
NVFBC_A4
NVFBC_CAS#
NVFBC_CAS# 58
NVFBC_CAS#
NVFBC_CAS# 58
NVFBC_CLK0
NVFBC_CLK0# 58
NVFBC_CLK1
NVFBC_CLK1# 58
NVFBC_CLK1# 58

NVFBC_CLK0
NVFBC_CLK0#
NVFBC_CLK1
NVFBC_CLK1#

RFU4
RFU5
FBC_DEBUG
FBC_REFCLK
FBC_REFCLKN

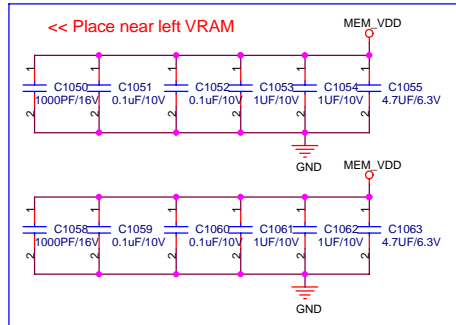
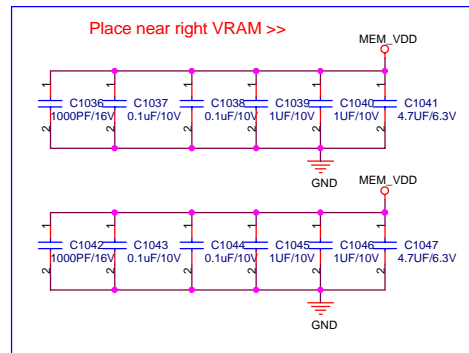
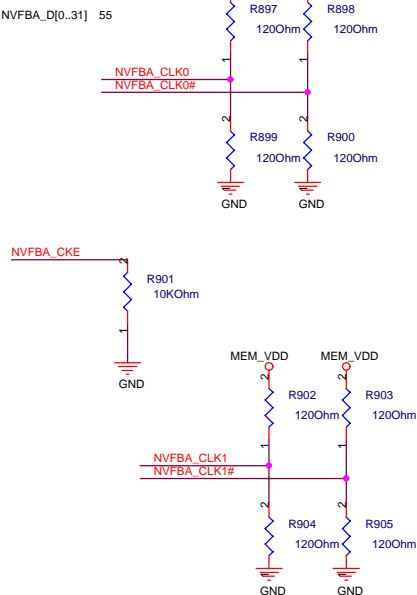
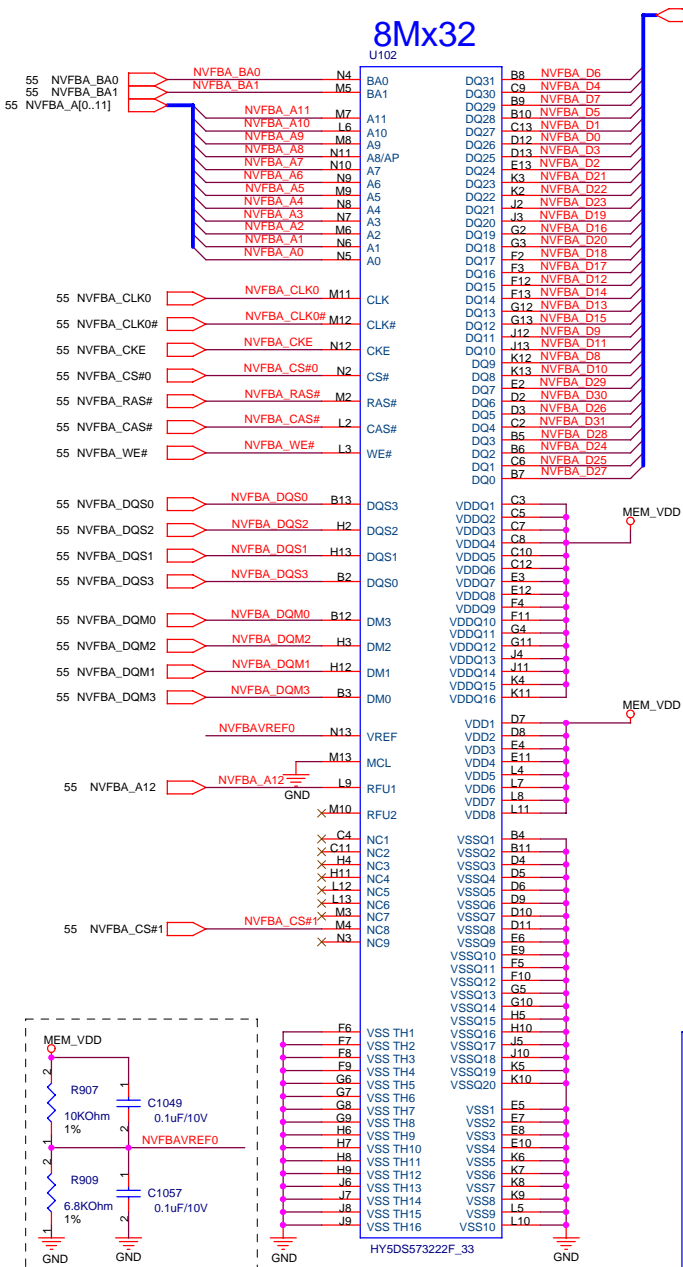
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FBC_PLLAVDD
FBC_PL LGND

FBCAL_PD_VDDQ
FBCAL_PU_GND
FBCAL_TERM_GND



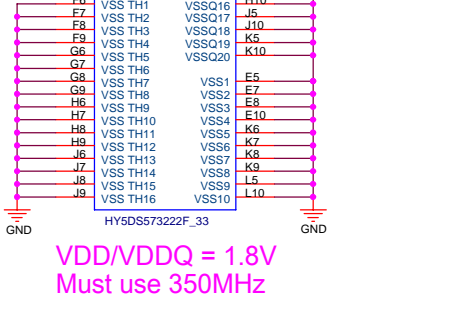
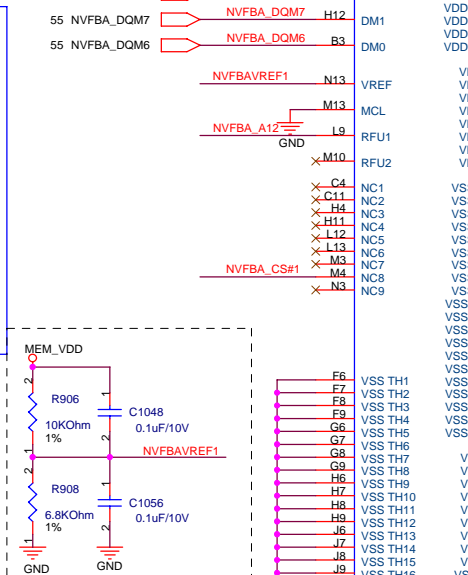
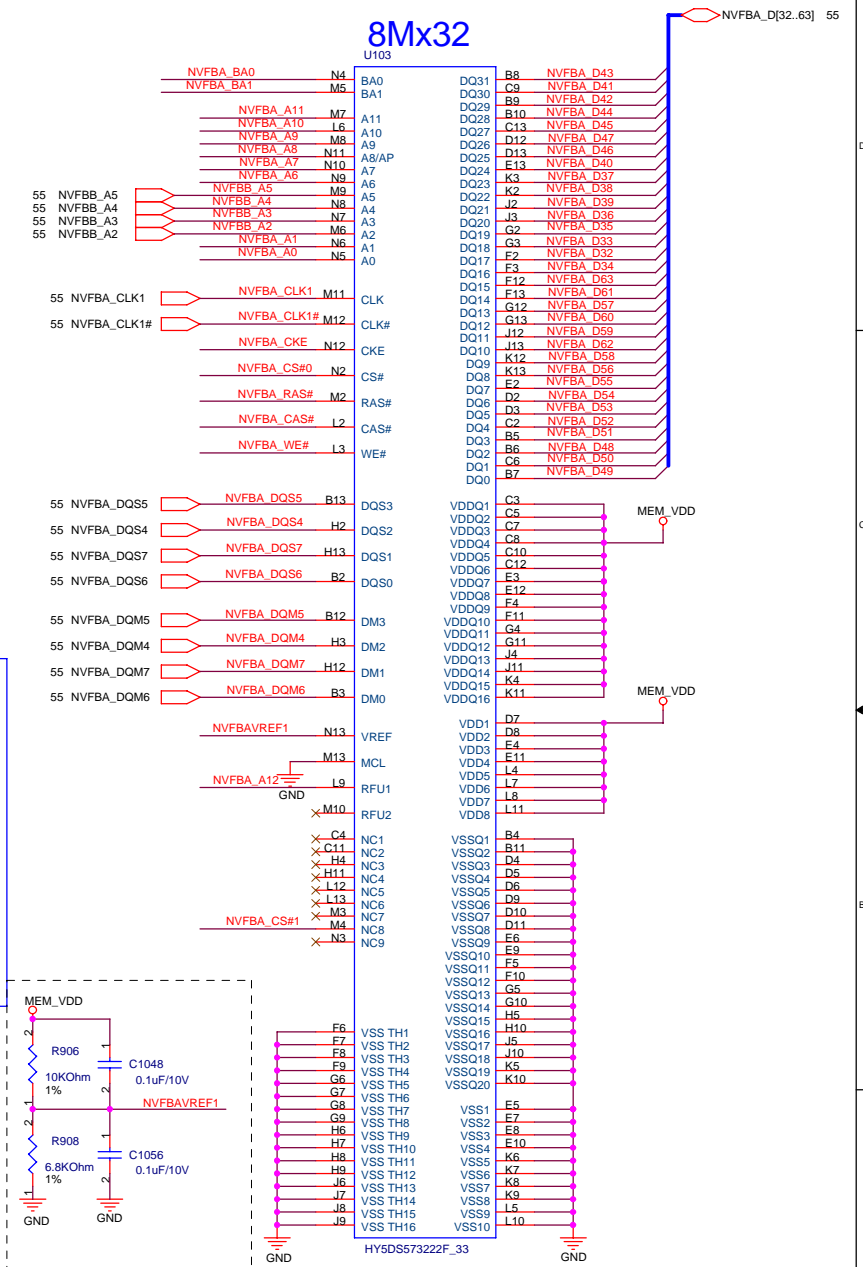
8Mx32

U102



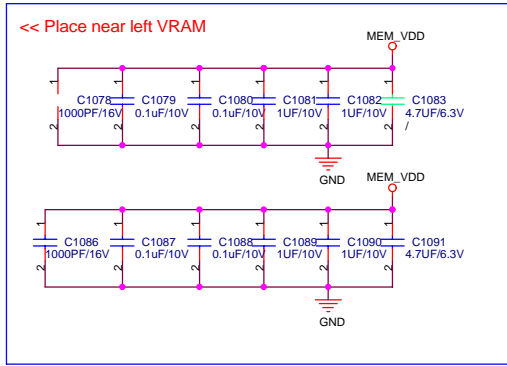
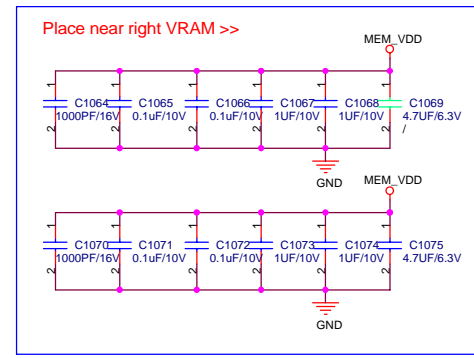
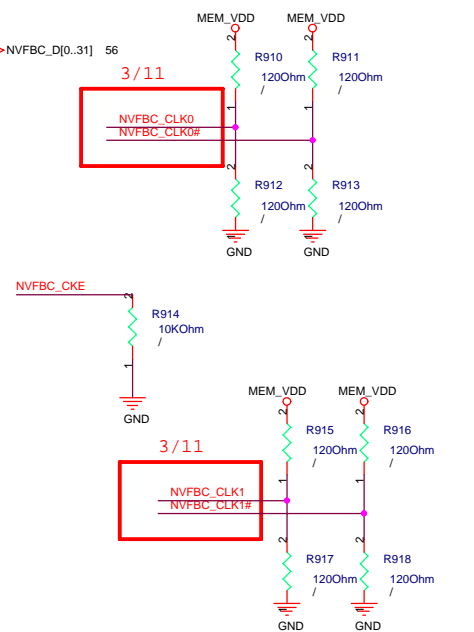
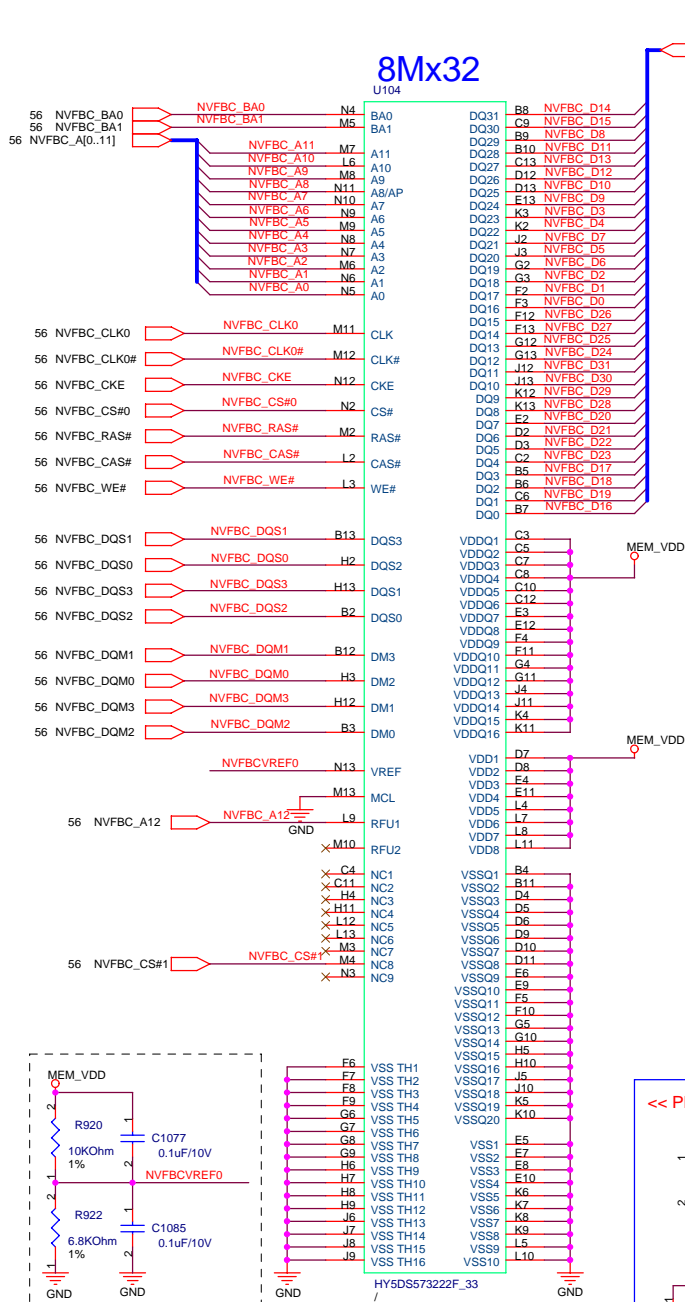
8Mx32

U103



8Mx32

U104



8Mx32

U105

